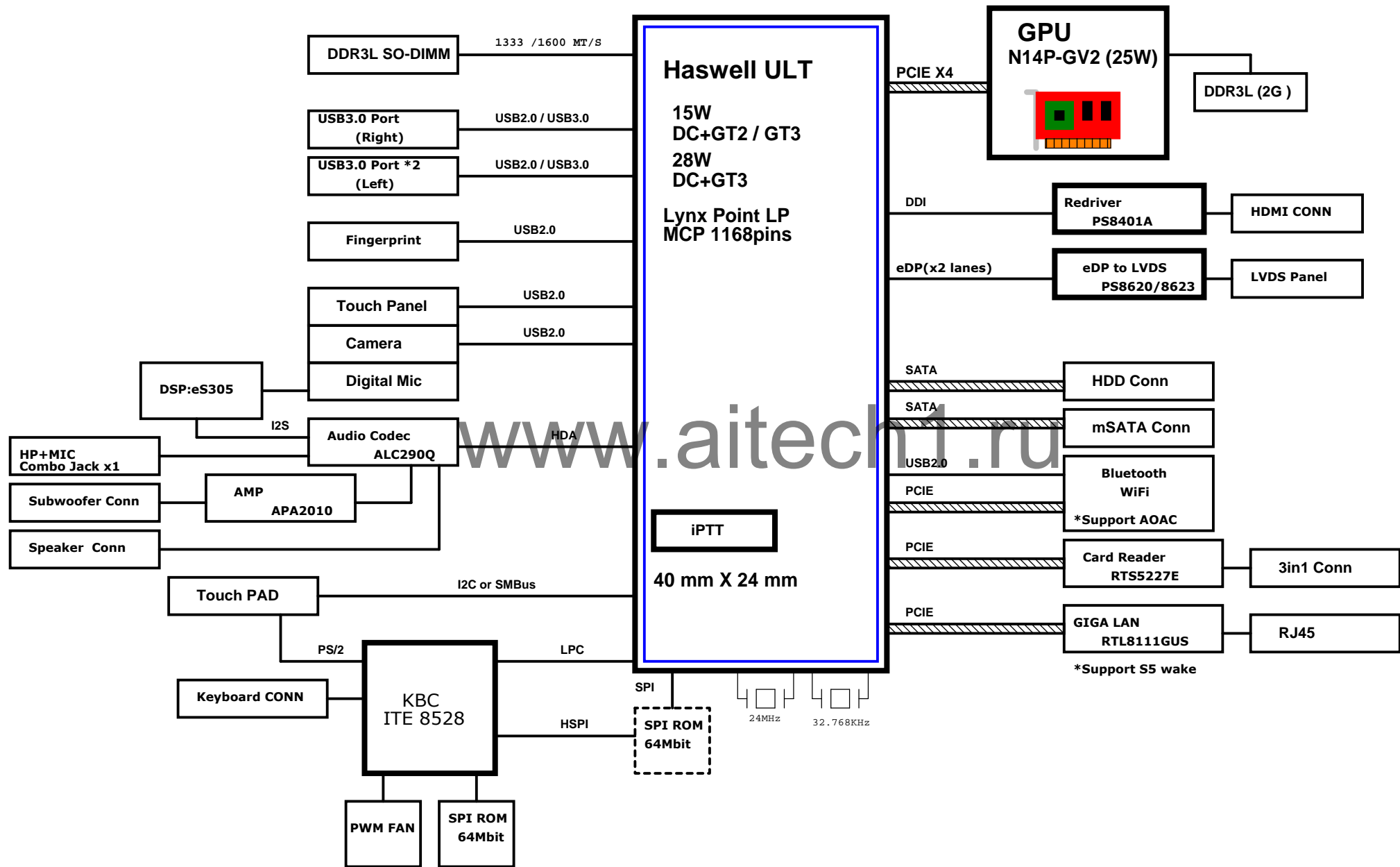


# JW8B/C BLOCK DIAGRAM

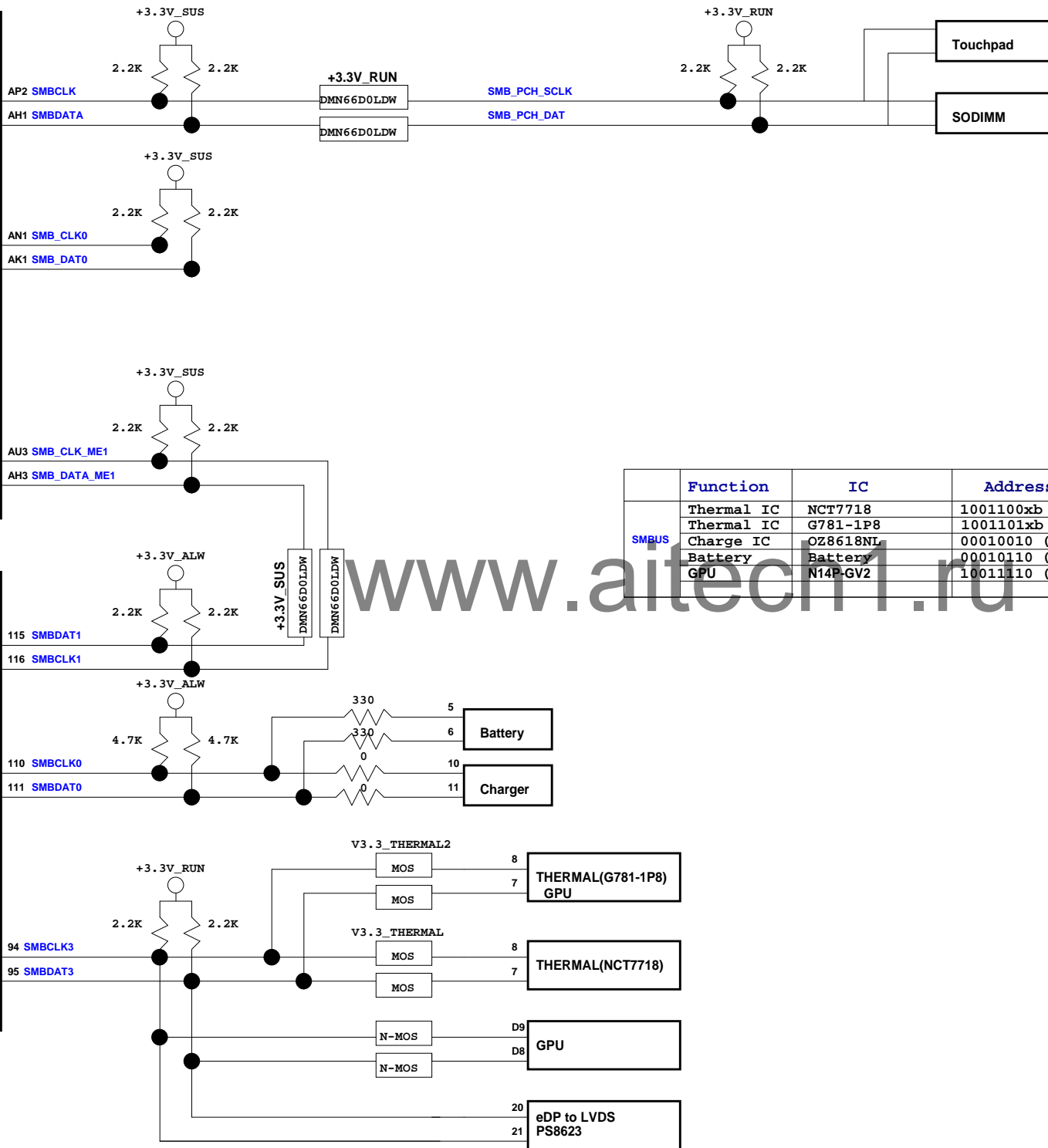
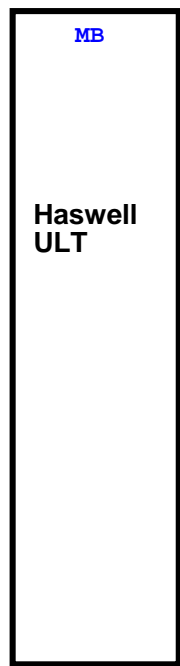


| HSIO Port | USB3.0          | PCIE                 | SATA           |
|-----------|-----------------|----------------------|----------------|
| 1         | USB3.0_1<br>CN6 |                      |                |
| 2         | USB3.0_2<br>CN4 |                      |                |
| 3         | USB3.0_3<br>CN5 | PCIE1<br>X           |                |
| 4         | USB3.0_4<br>X   | PCIE2<br>Card Reader |                |
| 5         |                 | PCIE3<br>GIGA LAN    |                |
| 6         |                 | PCIE4<br>WIFI        |                |
| 7         |                 | PCIE5<br>GPU 4X      |                |
| 8         |                 | PCIE5<br>GPU 4X      |                |
| 9         |                 | PCIE5<br>GPU 4X      |                |
| 10        |                 | PCIE5<br>GPU 4X      |                |
| 11        |                 | PCIE6<br>X           | SATA3<br>X     |
| 12        |                 | PCIE6<br>X           | SATA2<br>mSATA |
| 13        |                 | PCIE6<br>X           | SATA1<br>HDD   |
| 14        |                 | PCIE6<br>X           | SATA0<br>X     |

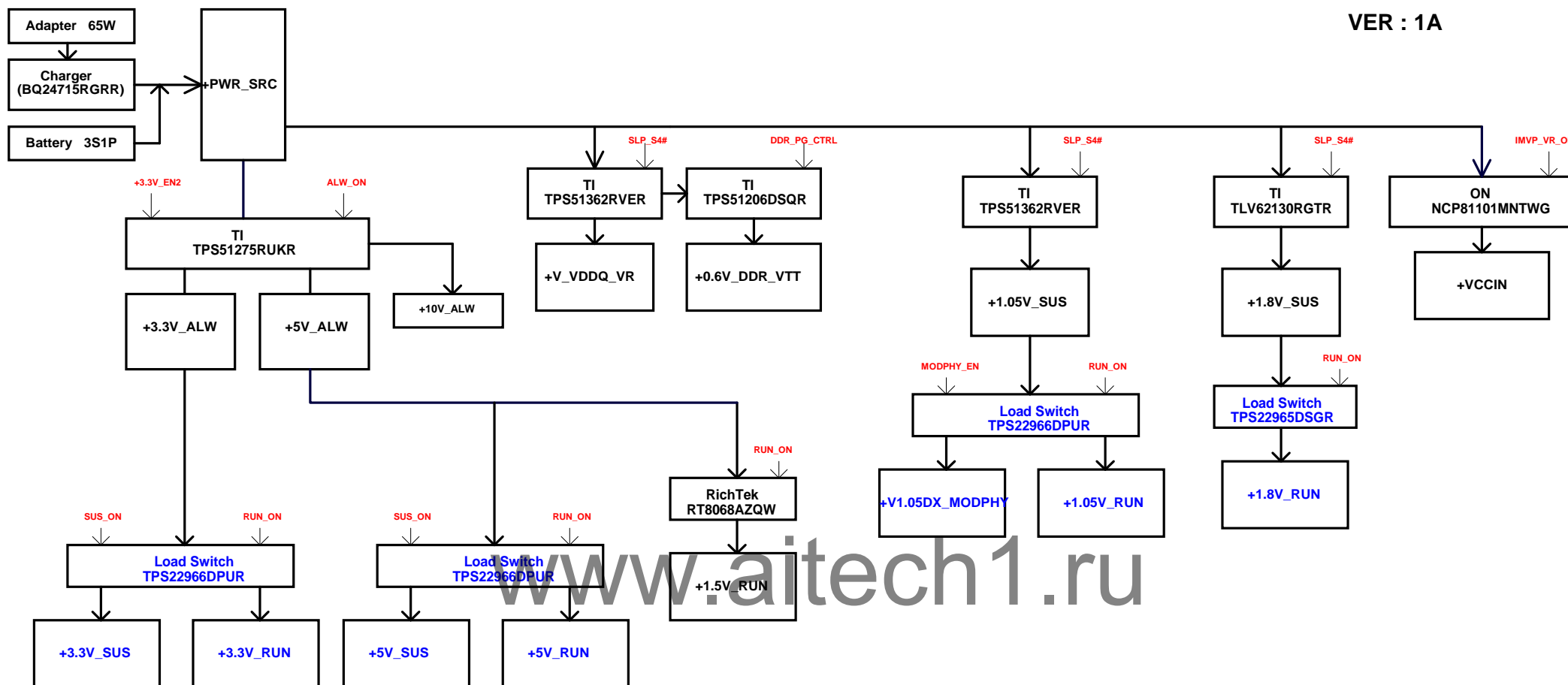
| PCIE CLK            |
|---------------------|
| CLK0<br>X           |
| CLK1<br>Card Reader |
| CLK2<br>GIGA LAN    |
| CLK3<br>WIFI        |
| CLK4<br>GPU 4X      |
| CLK5<br>X           |

| USB2.0                   |
|--------------------------|
| USB2.0_0<br>CN4          |
| USB2.0_1<br>CN6          |
| USB2.0_2<br>CN5          |
| USB2.0_3<br>Finger Print |
| USB2.0_4<br>Camera       |
| USB2.0_5<br>eTP          |
| USB2.0_6<br>Blue Tooth   |
| USB2.0_7<br>Touch Screen |

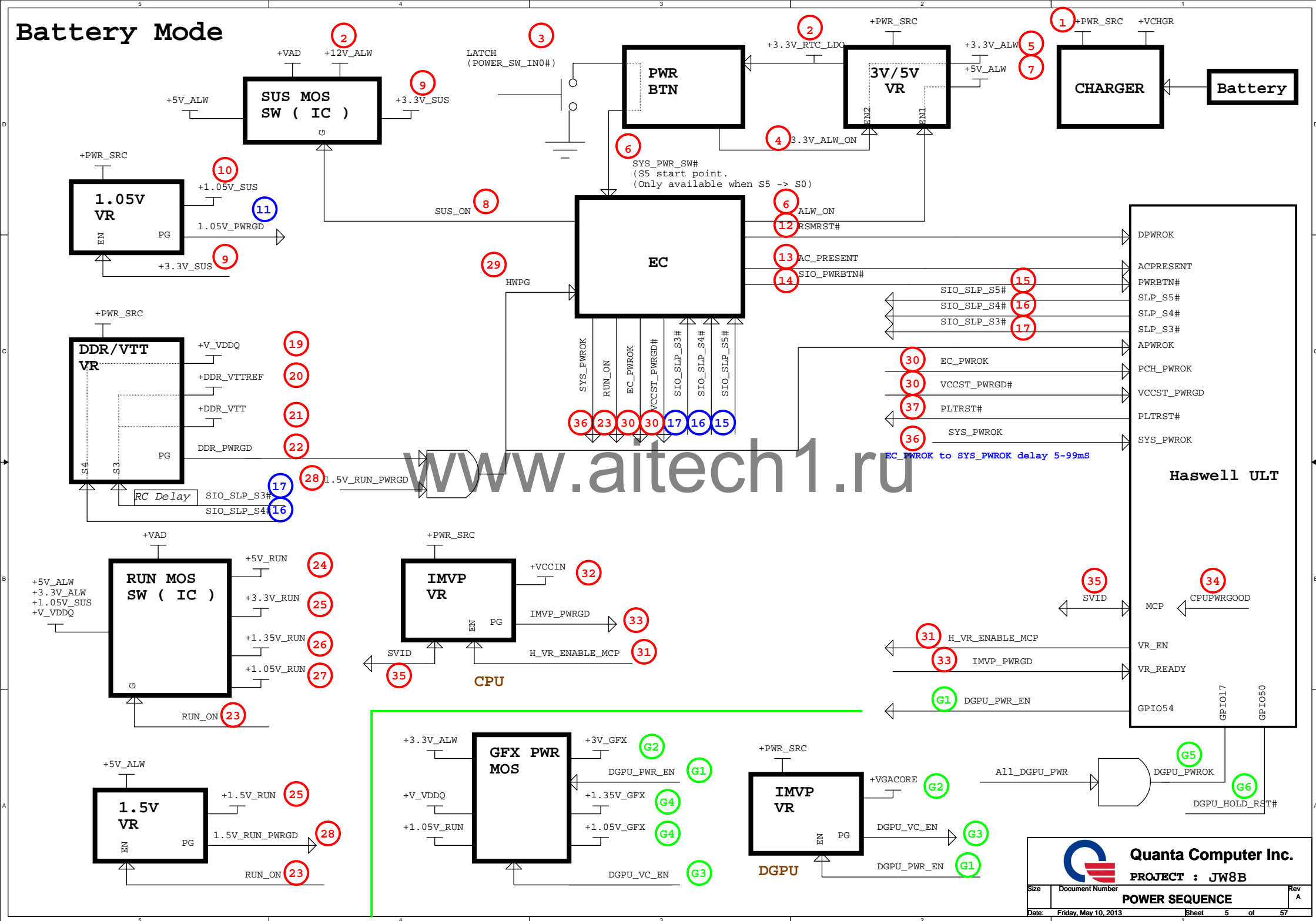
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|       | Function   | IC       | Address          |
|-------|------------|----------|------------------|
| SMBUS | Thermal IC | NCT7718  | 1001100xb (98h)  |
|       | Thermal IC | G781-1P8 | 1001101xb (9Ah)  |
|       | Charge IC  | OZ8618NL | 00010010 (0x12h) |
|       | Battery    | Battery  | 00010110 (0X16h) |
|       | GPU        | N14P-GV2 | 10011110 (0X9Eh) |
|       |            |          |                  |

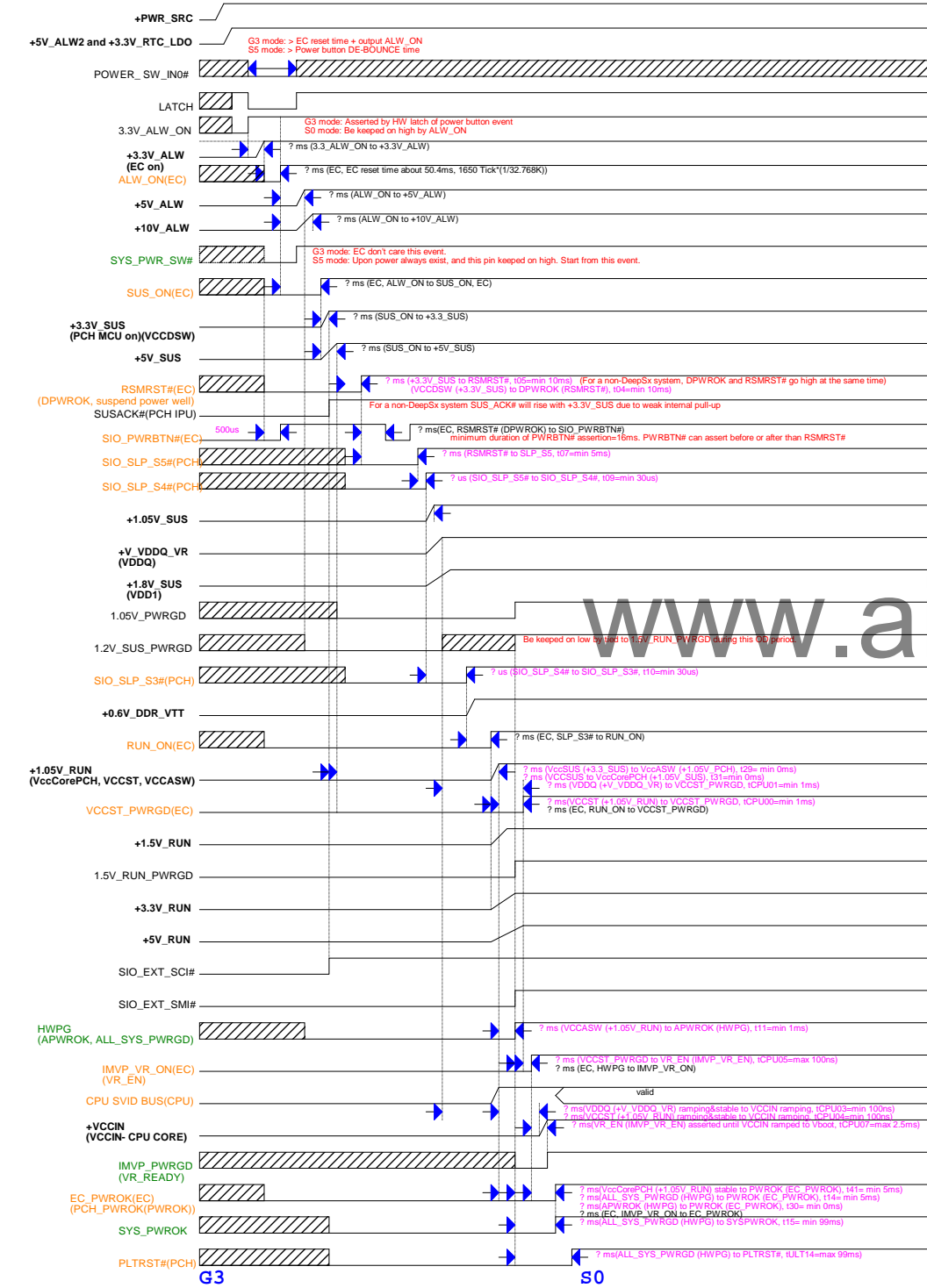


## Battery Mode

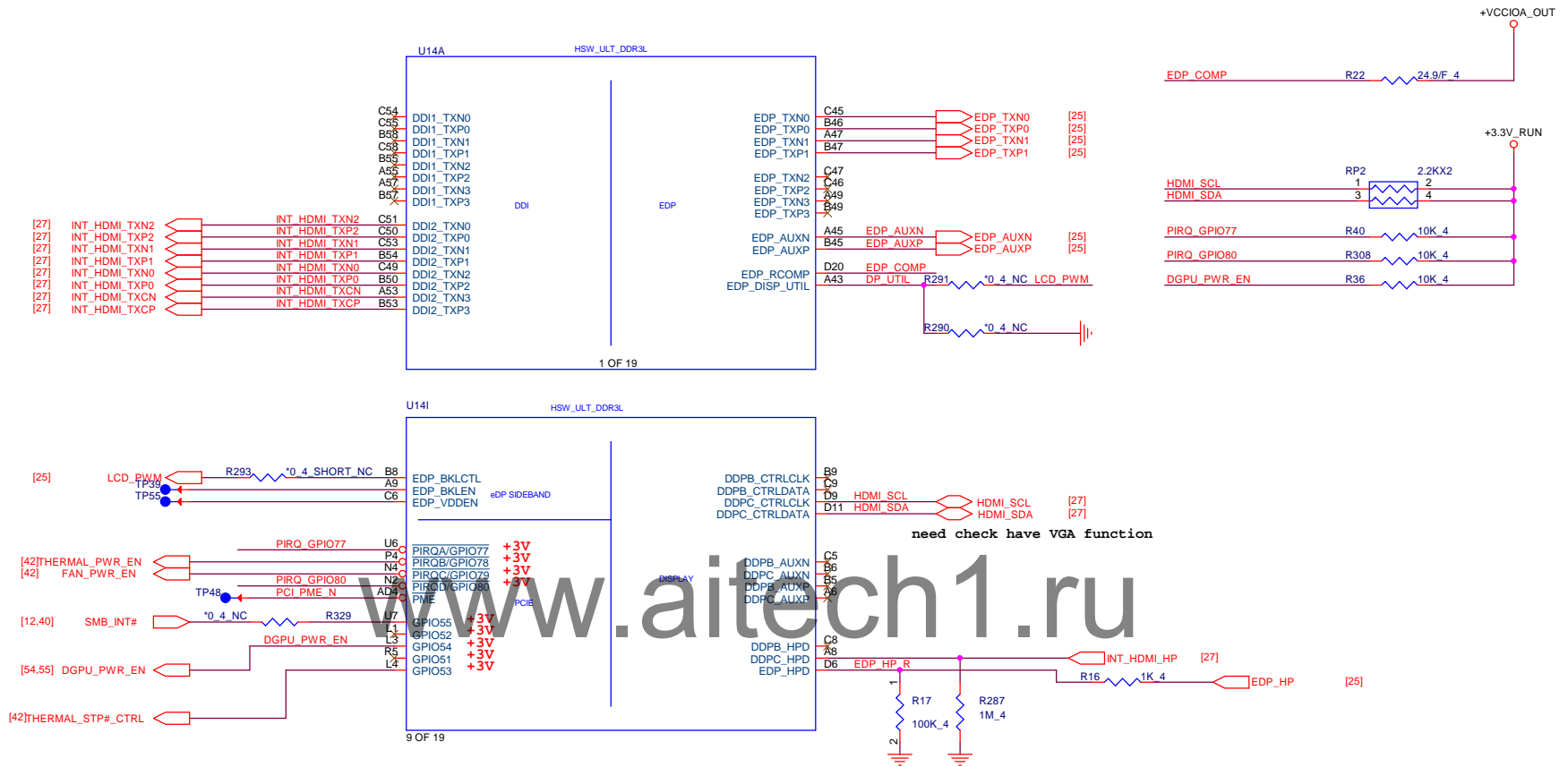


Power Sequence  
(G3 to S0)

Shark Bay ULT PSS, 490828, Rev1.1



# Haswell ULT (DISPLAY)



Quanta Computer Inc.

PROJECT : JW8B

|       |                        |               |
|-------|------------------------|---------------|
| Size  | Document Number        | Rev           |
|       | Haswell ULT 1/12       | A             |
| Date: | Tuesday, July 16, 2013 | Sheet 7 of 57 |

# Haswell ULT (DDR3L)

U14C

HSW\_ULT\_DDR3L

|         |          |      |
|---------|----------|------|
| AH63    | SA_DQ0   | AU37 |
| AH62    | SA_DQ1   | AW37 |
| AK63    | SA_CLK#0 | AW36 |
| AK62    | SA_CLK#1 | AY36 |
| AH61    | SA_CLK1  |      |
| AH60    | SA_DQ4   | AU43 |
| SA_DQ5  | SA_CKE0  | AW43 |
| AK61    | SA_CKE1  | AY42 |
| AK60    | SA_DQ7   | AY43 |
| AM63    | SA_DQ8   |      |
| AM62    | SA_CKE2  | AP33 |
| AP63    | SA_CKE3  | AR32 |
| AP62    | SA_CS#0  |      |
| AM61    | SA_CS#1  | AP32 |
| AM60    | SA_ODT0  |      |
| AP61    |          | AY34 |
| AP60    | SA_RAS   | AW34 |
| AP59    | SA_WE    | AY34 |
| AP58    | SA_CAS   |      |
| AR58    |          | AU35 |
| AM57    | SA_BA0   | AV35 |
| AK57    | SA_BA1   | AY41 |
| AL58    | SA_BA2   |      |
| AK58    |          | AU36 |
| AR57    |          | AY37 |
| AN57    | SA_MA0   | AR38 |
| AP58    | SA_MA1   | AP36 |
| AR56    | SA_MA2   | AU39 |
| AM54    | SA_MA3   | AR36 |
| AK54    | SA_MA4   | AY40 |
| AL55    | SA_MA5   | AW39 |
| AK55    | SA_MA6   | AY39 |
| AR54    | SA_MA7   | AU40 |
| AN54    | SA_MA8   | AP35 |
| AY58    | SA_MA9   | AW41 |
| AY56    | SA_MA10  | AU41 |
| AW58    | SA_MA11  | AR35 |
| AW56    | SA_MA12  | AY42 |
| AV58    | SA_MA13  | AU42 |
| AU58    | SA_MA14  |      |
| AV56    | SA_MA15  |      |
| AU56    |          | AJ61 |
| AY54    | SA_DQSN0 | AN62 |
| AW54    | SA_DQSN1 | AN62 |
| AY52    | SA_DQSN2 | AW58 |
| AW52    | SA_DQSN3 | AM55 |
| AV54    | SA_DQSN4 | AV57 |
| AU54    | SA_DQSN5 | AV53 |
| AV52    | SA_DQSN6 | AL43 |
| AU52    | SA_DQSN7 | AL43 |
| AK49    |          | AL48 |
| AK42    |          | AJ62 |
| AM43    | SA_DQSP0 | AN61 |
| AM45    | SA_DQSP1 | AN58 |
| AK45    | SA_DQSP2 | AN58 |
| AK43    | SA_DQSP3 | AN55 |
| AM40    | SA_DQSP4 | AW57 |
| AM42    | SA_DQSP5 | AW53 |
| AM46    | SA_DQSP6 | AL42 |
| AK46    | SA_DQSP7 | AL49 |
| SA_DQ57 |          |      |
| SA_DQ58 |          |      |
| SA_DQ59 |          |      |
| SA_DQ60 |          |      |
| SA_DQ61 |          |      |
| SA_DQ62 |          |      |
| SA_DQ63 |          |      |

DDR CHANNEL A

3 OF 19

[19] M\_B\_DQ[63..0]

U14D

HSW\_ULT\_DDR3L

|          |      |
|----------|------|
| M_B_DQ0  | AY31 |
| M_B_DQ1  | AW31 |
| M_B_DQ2  | AY29 |
| M_B_DQ3  | AW29 |
| M_B_DQ4  | AV31 |
| M_B_DQ5  | AU31 |
| M_B_DQ6  | AV29 |
| M_B_DQ7  | AU29 |
| M_B_DQ8  | AY27 |
| M_B_DQ9  | AW27 |
| M_B_DQ10 | AY25 |
| M_B_DQ11 | AW25 |
| M_B_DQ12 | AV27 |
| M_B_DQ13 | AU27 |
| M_B_DQ14 | AV25 |
| M_B_DQ15 | AU25 |
| M_B_DQ16 | AM29 |
| M_B_DQ17 | AK29 |
| M_B_DQ18 | AL28 |
| M_B_DQ19 | AK28 |
| M_B_DQ20 | AR29 |
| M_B_DQ21 | AN29 |
| M_B_DQ22 | AR28 |
| M_B_DQ23 | AP28 |
| M_B_DQ24 | AN26 |
| M_B_DQ25 | AR26 |
| M_B_DQ26 | AR25 |
| M_B_DQ27 | AP25 |
| M_B_DQ28 | AK26 |
| M_B_DQ29 | AM26 |
| M_B_DQ30 | AK25 |
| M_B_DQ31 | AL25 |
| M_B_DQ32 | AY23 |
| M_B_DQ33 | AW23 |
| M_B_DQ34 | AY21 |
| M_B_DQ35 | AW21 |
| M_B_DQ36 | AV23 |
| M_B_DQ37 | AU23 |
| M_B_DQ38 | AV21 |
| M_B_DQ39 | AU21 |
| M_B_DQ40 | AY19 |
| M_B_DQ41 | AW19 |
| M_B_DQ42 | AY17 |
| M_B_DQ43 | AW17 |
| M_B_DQ44 | AV19 |
| M_B_DQ45 | AL19 |
| M_B_DQ46 | AV17 |
| M_B_DQ47 | AU17 |
| M_B_DQ48 | AR21 |
| M_B_DQ49 | AR22 |
| M_B_DQ50 | AL21 |
| M_B_DQ51 | AM22 |
| M_B_DQ52 | AN22 |
| M_B_DQ53 | AP21 |
| M_B_DQ54 | AK21 |
| M_B_DQ55 | AK22 |
| M_B_DQ56 | AN20 |
| M_B_DQ57 | AR20 |
| M_B_DQ58 | AK18 |
| M_B_DQ59 | AL18 |
| M_B_DQ60 | AK20 |
| M_B_DQ61 | AM20 |
| M_B_DQ62 | AR18 |
| M_B_DQ63 | AP18 |

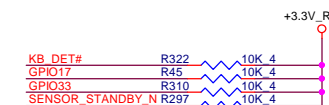
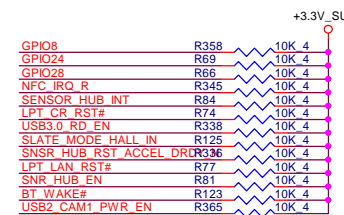
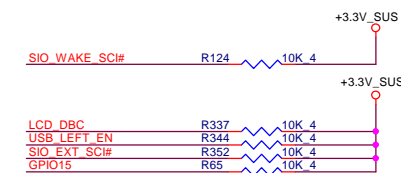
DDR CHANNEL B

4 OF 19

Check if not used. NC ?  
12/25 Del SM\_VREF\_DQ0

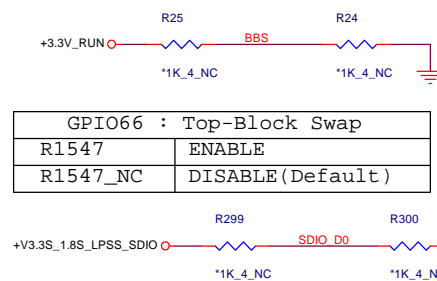


### **GPIO Pull-up/Pull-down(CLG)**



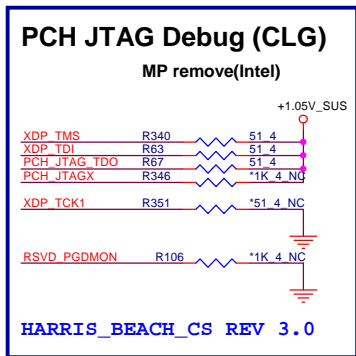
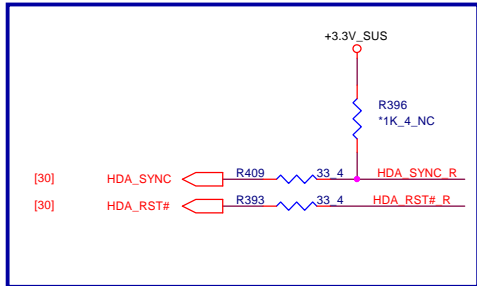
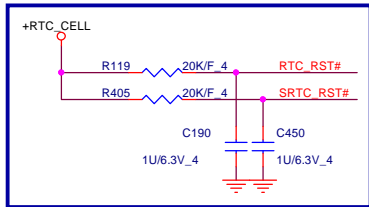
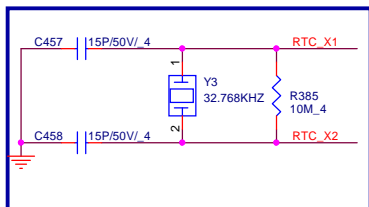
| GPIO86:Boot BIOS Strap Bit |                   |
|----------------------------|-------------------|
| PU                         | LPC               |
| PD                         | SPI (Default IPD) |

|                         |                  |
|-------------------------|------------------|
| GPIO66 : Top-Block Swap |                  |
| R1547                   | ENABLE           |
| R1547_NC                | DISABLE(Default) |



## 14K HSW\_ULT\_DDR3U



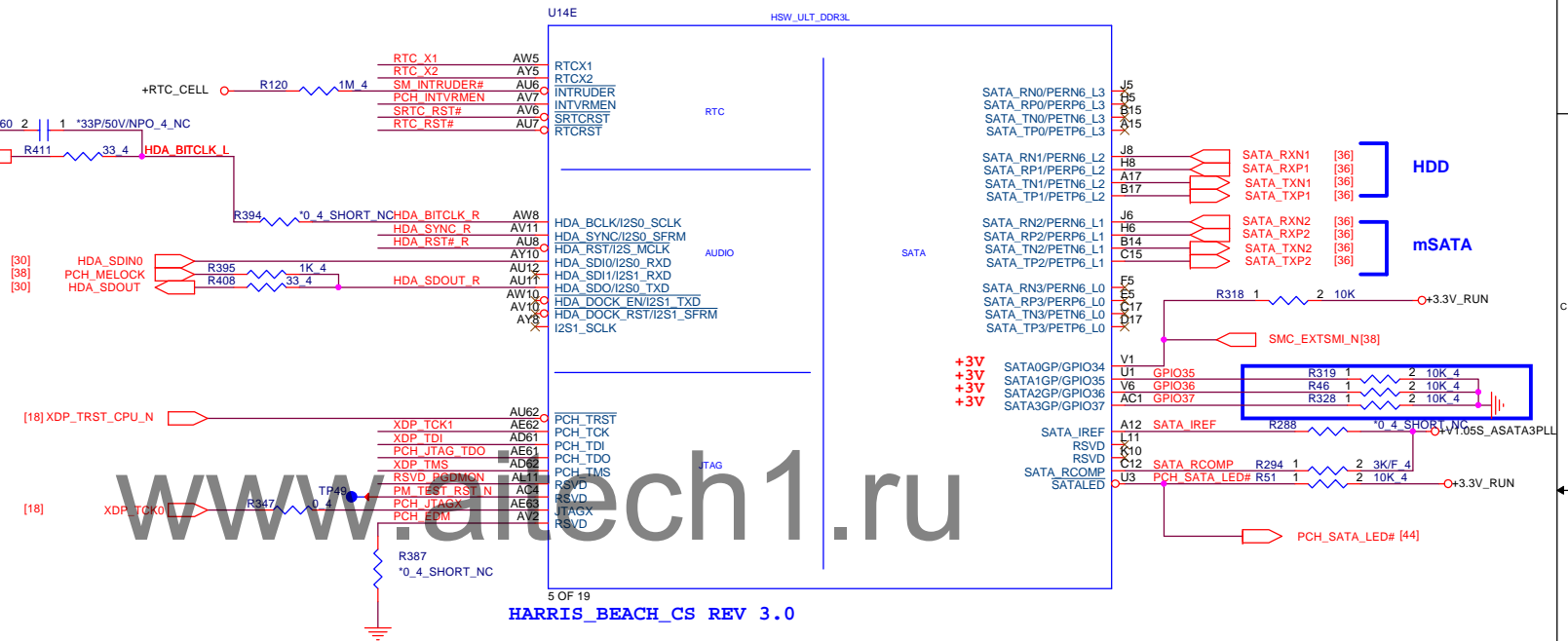


DFXTESTMODE  
HIGH - DFXTESTMODE DISABLED(DEFAULT)  
LOW - DFXTESTMODE ENABLED

PCH Strap Table

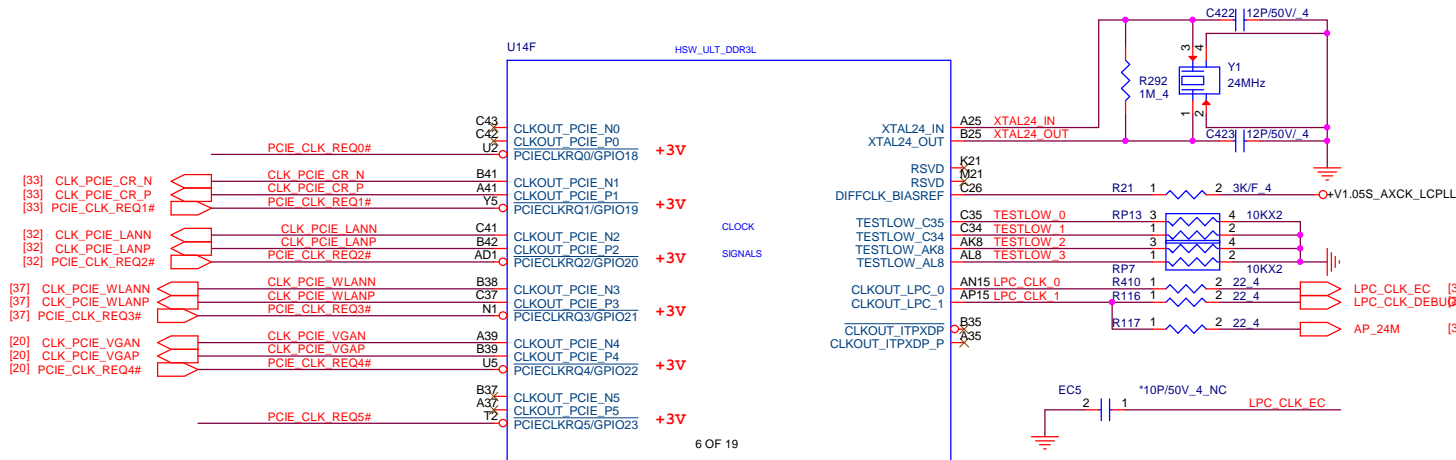
| Pin Name | Strap description   | Sampled | Configuration   | note  |
|----------|---|---------|---|---|
| SPKR     | No reboot mode setting                                      | PWROK   | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode |   |
| HDA_SDO  | Flash Descriptor Security<br>Override / Intel ME Debug Mode | PWROK   | 0 = Security Effect (Int PD)<br>1 = Can be Override               |   |
| INTVRMEN | Integrated 1.05V VRM enable                                 | ALWAYS  | Should be always pull-up  | +RTC_CELL R407 330K 4 NC PCH_INTVRMEN R392 330K 4 |

## Haswell ULT (RTC, HDA, JTAG, SATA)

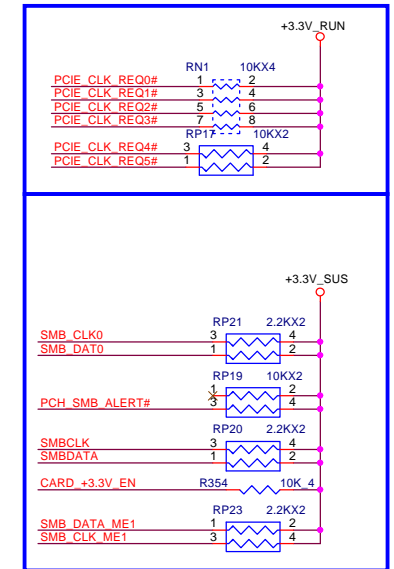
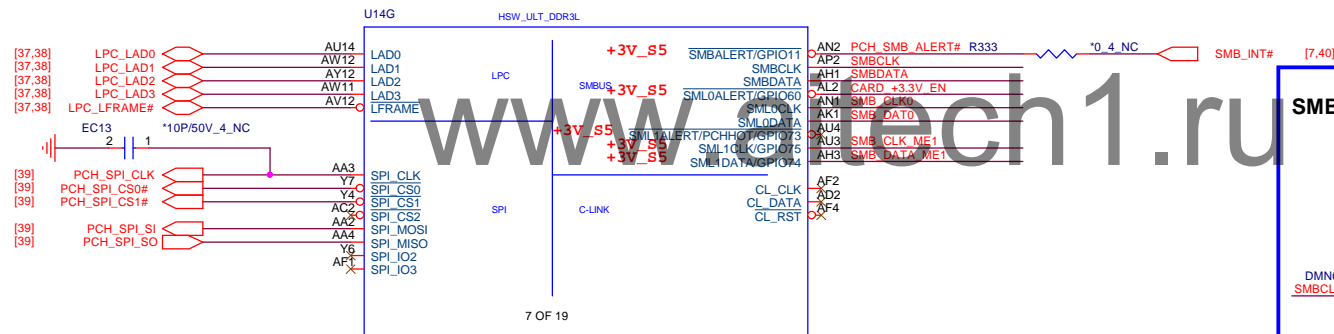


HARRIS\_BEACH\_CS REV 3.0

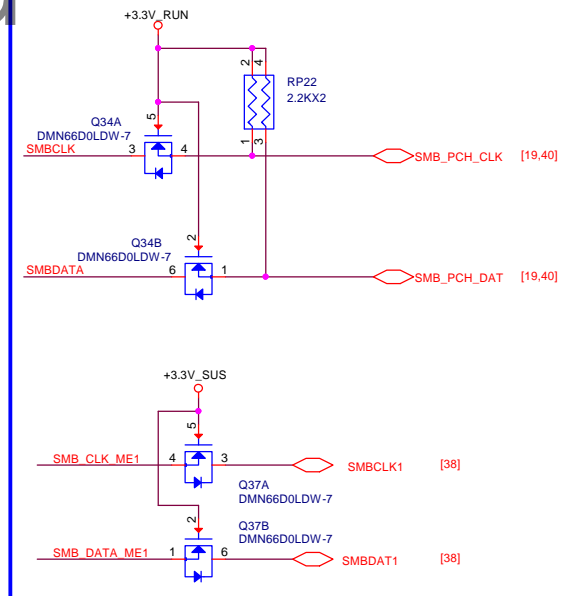
## Haswell ULT (CLK)



## Haswell ULT (LPC/SPI/SMB/CLINK)

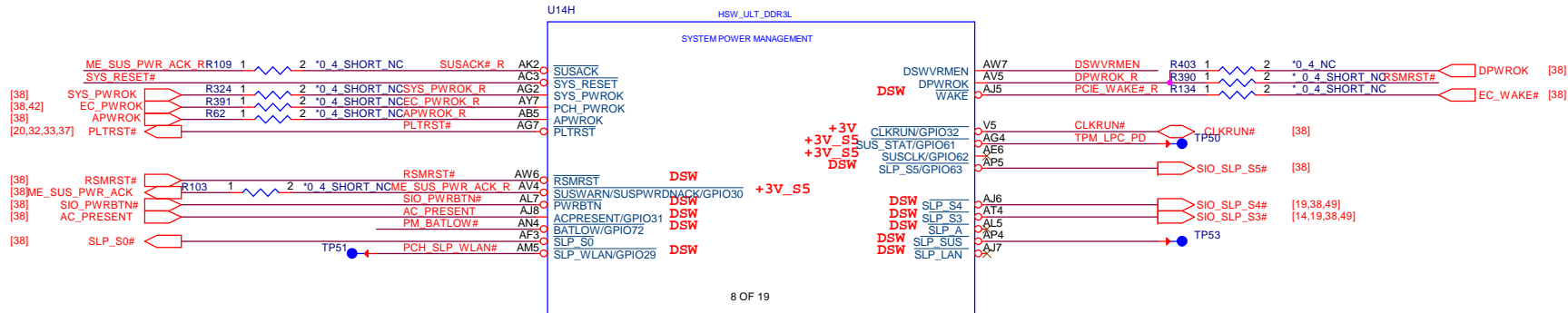


## SMBus/Pull-up (CLG)

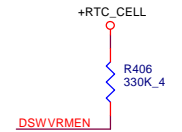
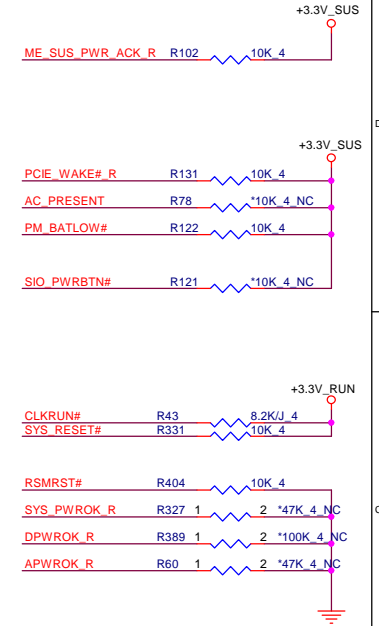


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PROJECT : JW8B

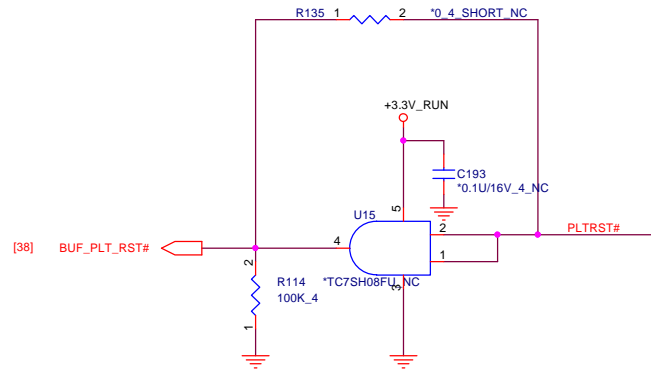
# Haswell ULT (SYSTEM POWER MANAGEMENT)



## PCH Pull-high/low(CLG)



On Die DSW VR Enable  
High = Enable (Default)  
Low = Disable



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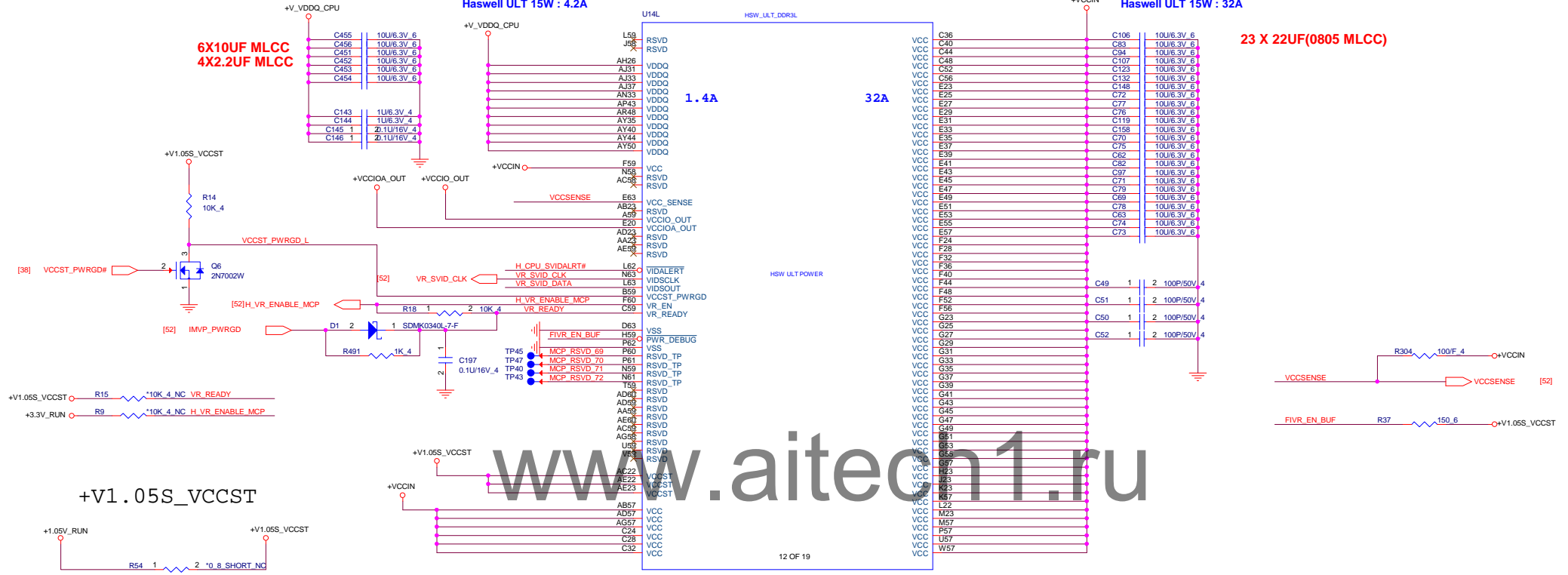
# Haswell ULT MCP (POWER)

**CPU VDDQ**  
Haswell ULT 15W : 4.2A

**CPU VCC** 1/21: 220uX23 --> 100uX23  
Haswell ULT 15W : 32A

6X10UF MLCC  
4X2.2UF MLCC

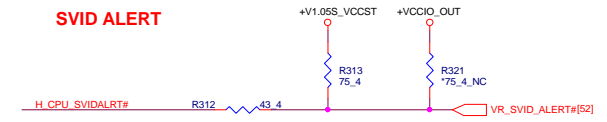
23 X 22UF(0805 MLCC)



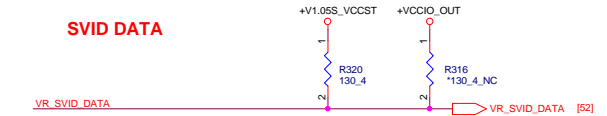
**S3 Power reduce**



**SVID ALERT**



**SVID DATA**



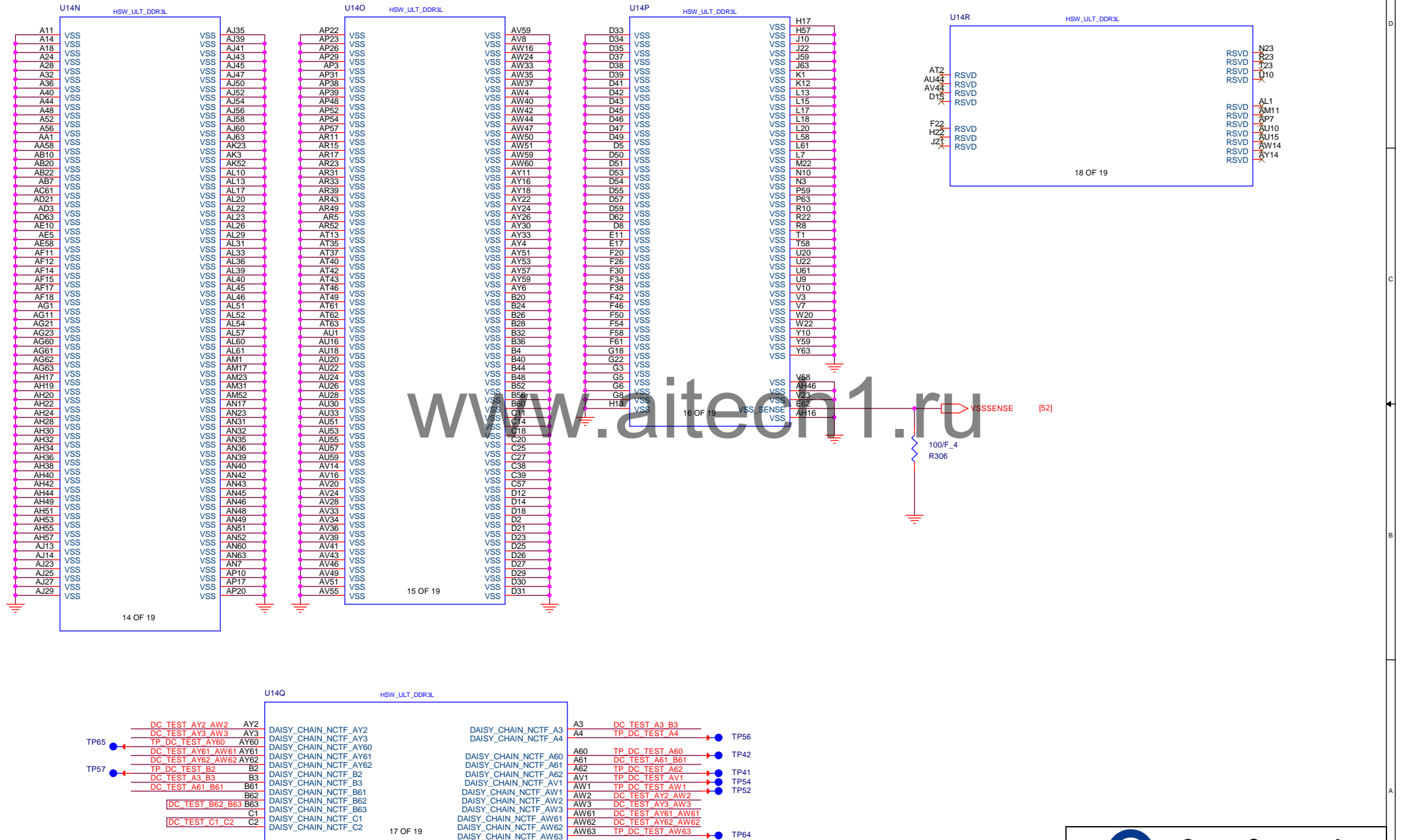
**Quanta Computer Inc.**

**PROJECT : JW8B**

**Haswell ULT 8/12**

| Size                        | Document Number | Rev |
|-----------------------------|-----------------|-----|
|                             |                 | A   |
| Date: Monday, July 08, 2013 | Sheet 14 of 57  |     |

# Haswell ULT (GND)

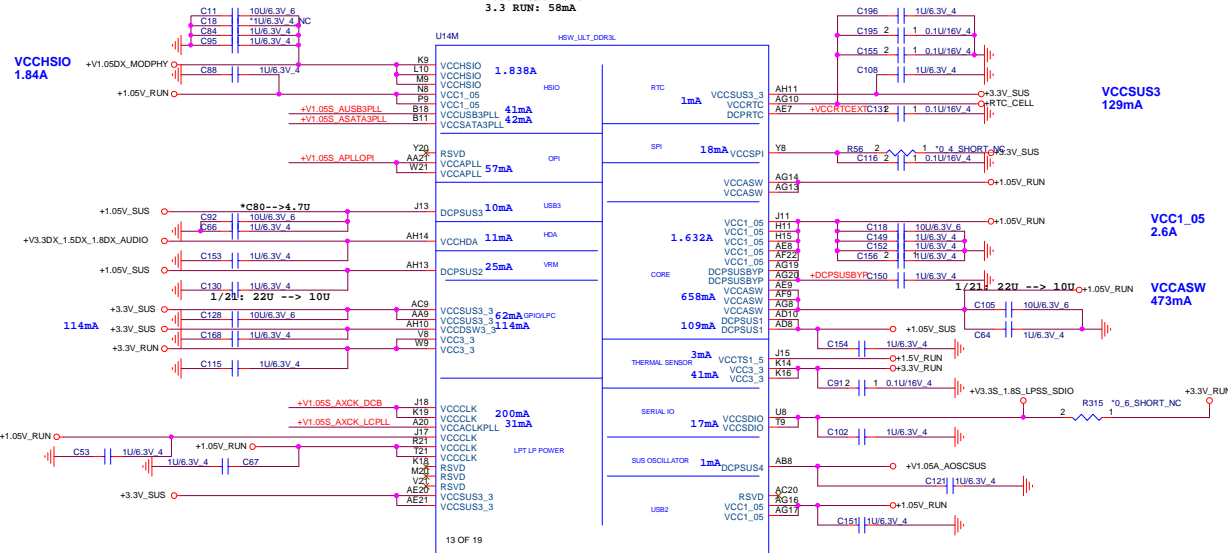




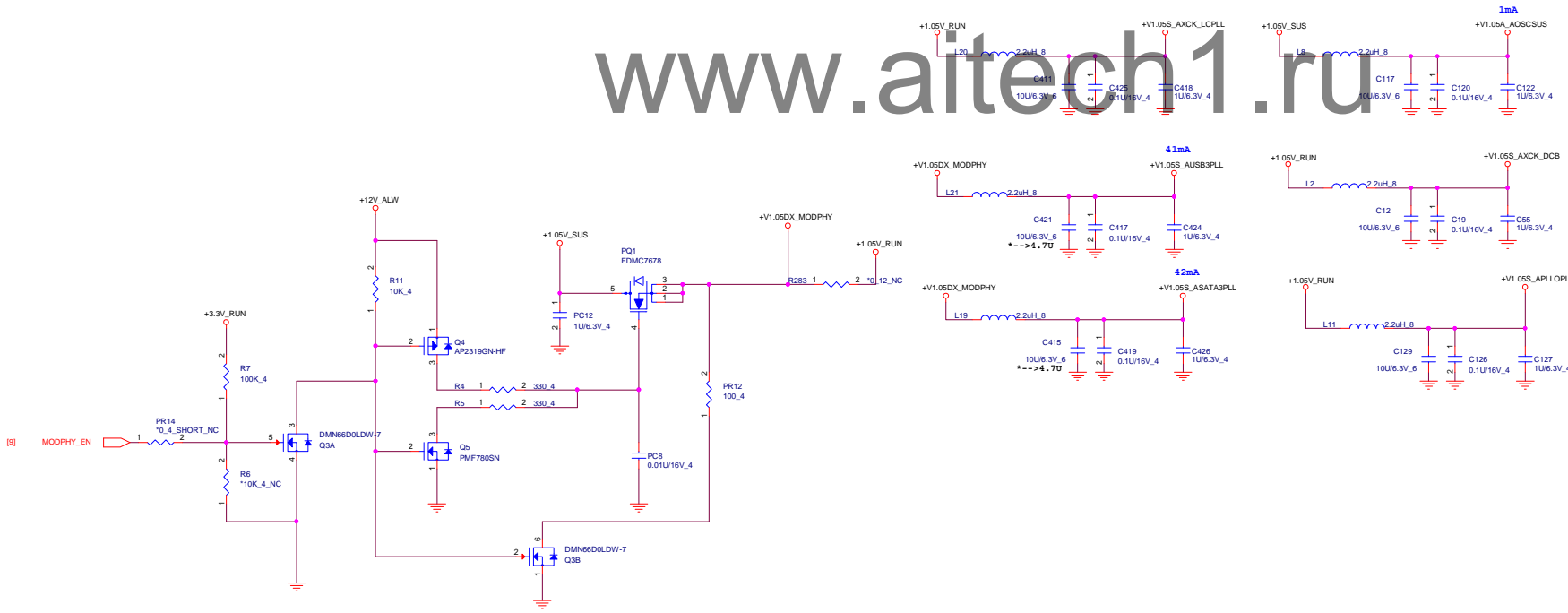


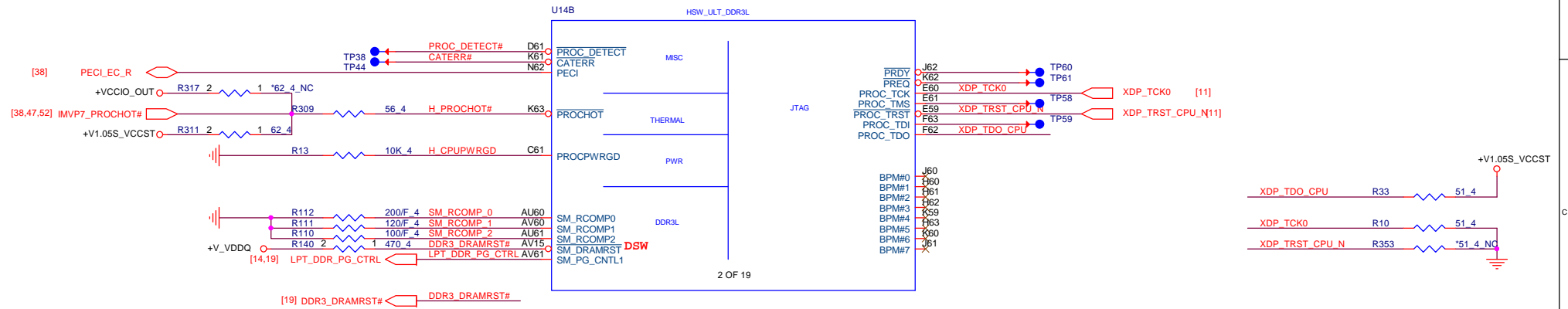
# Haswell ULT PCH(POWER)

3.3 SUS: 205mA  
1.05 SUS: 206mA  
1.05 RUN: 257mA  
3.3 RUN: 58mA



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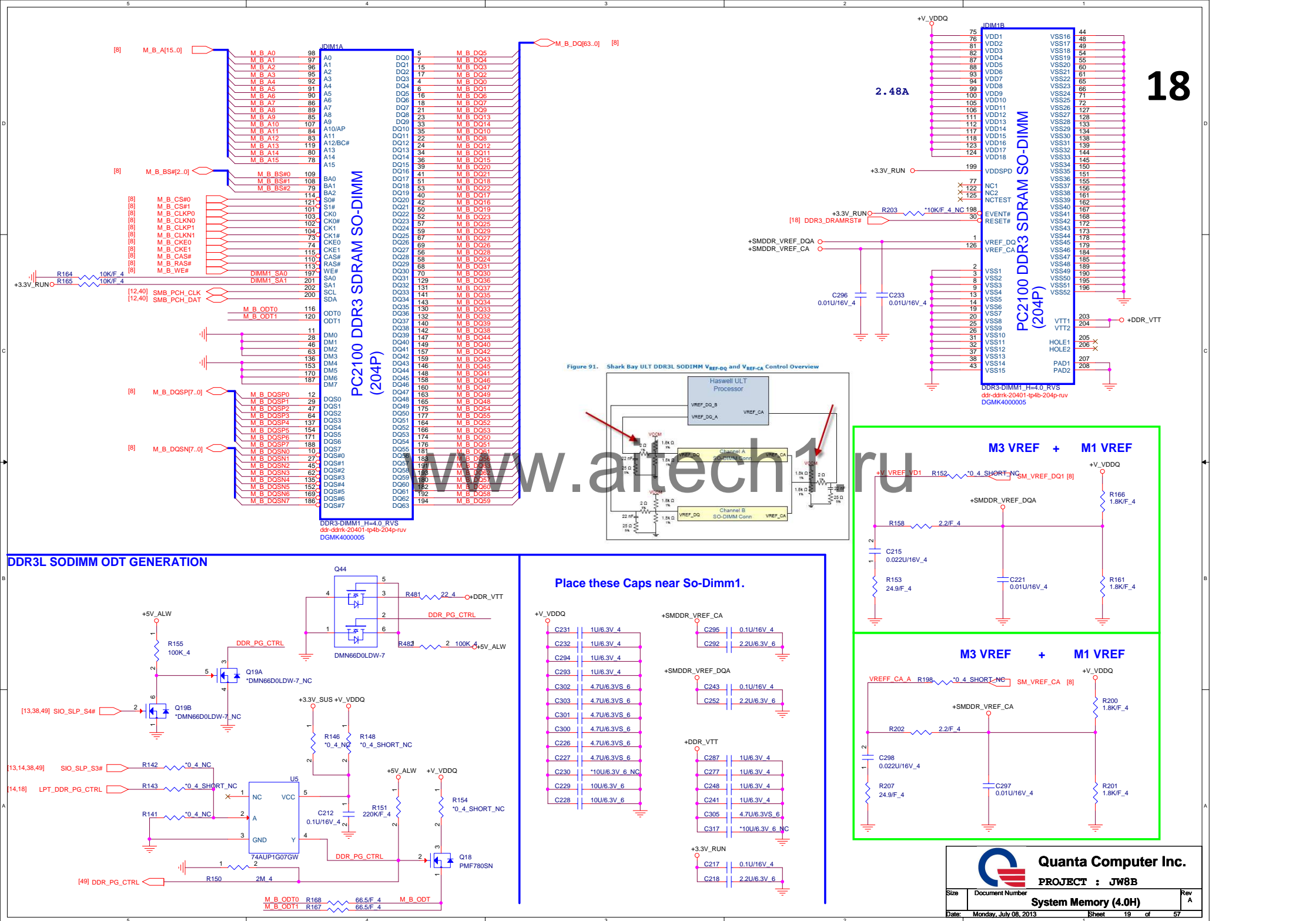
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Quanta Computer Inc.

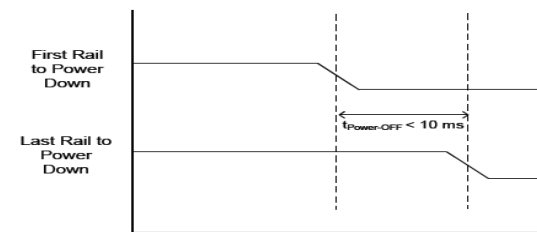
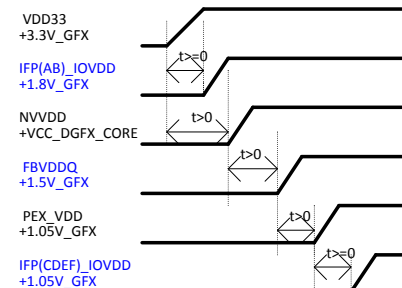
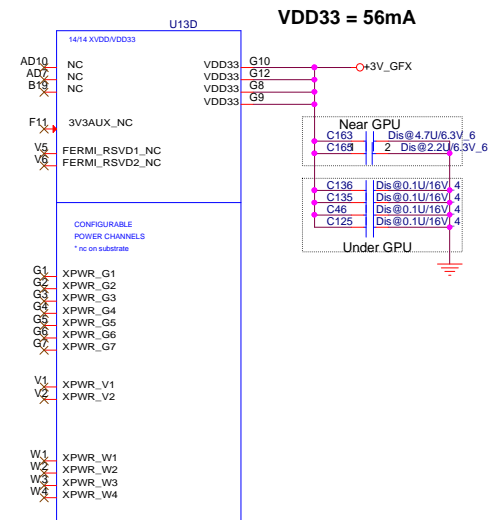
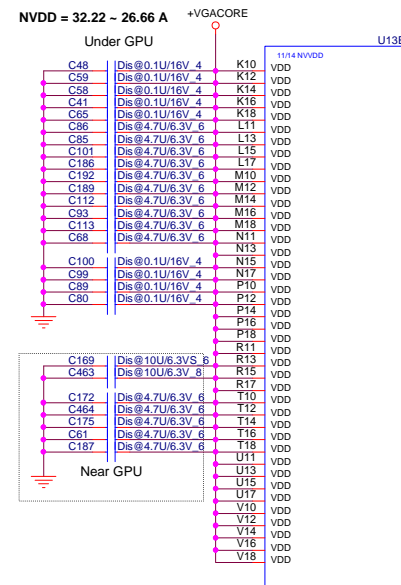
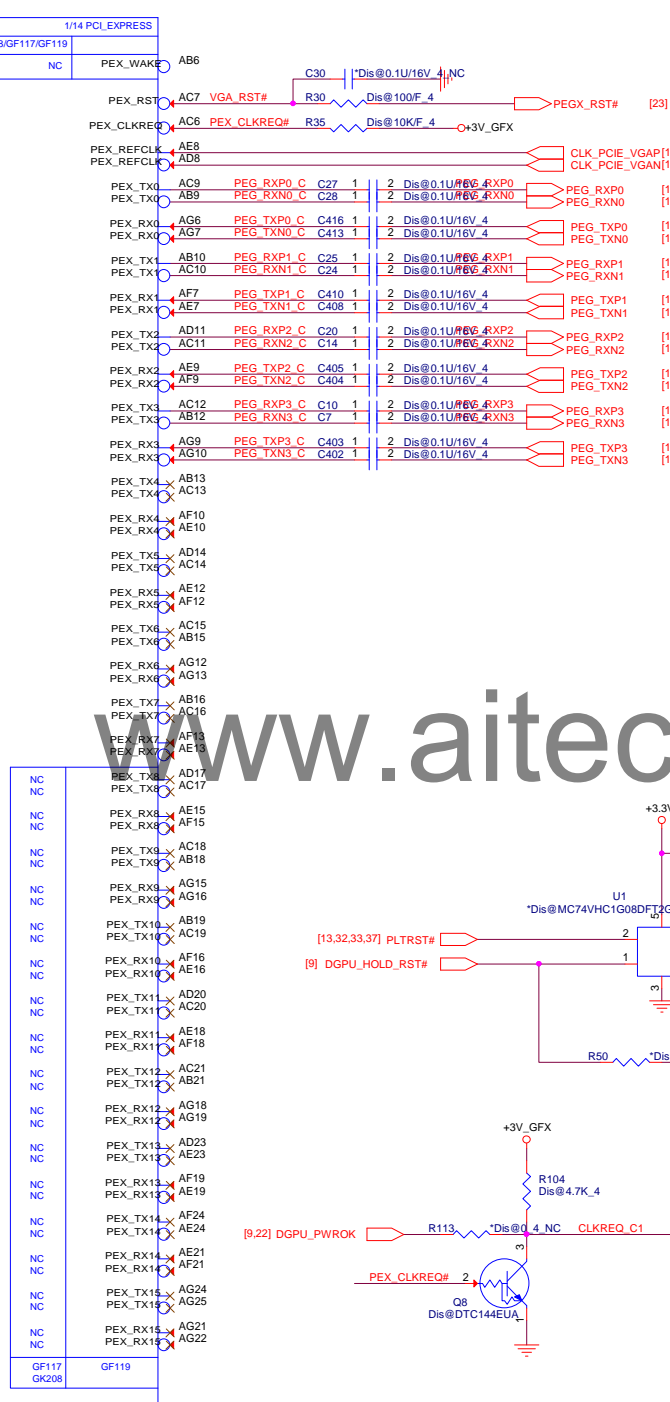
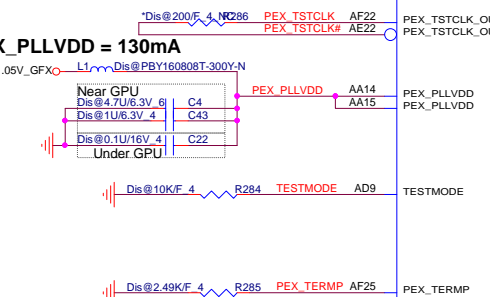
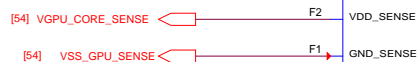
PROJECT : JW8B

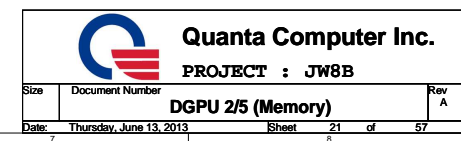
|       |                      |                |
|-------|----------------------|----------------|
| Size  | Document Number      | Rev A          |
| Date: | Friday, May 10, 2013 | Sheet 18 of 57 |



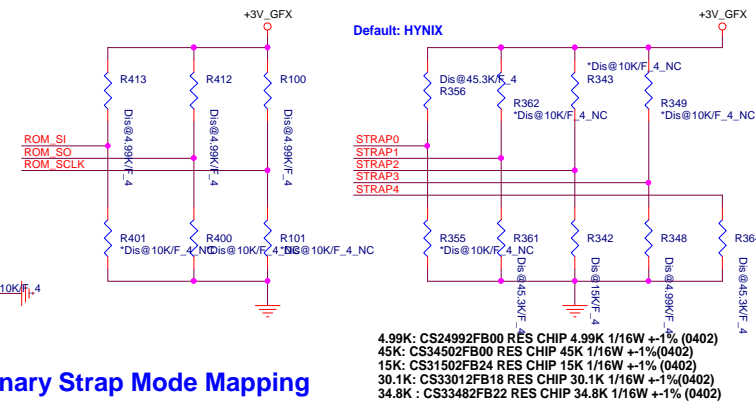
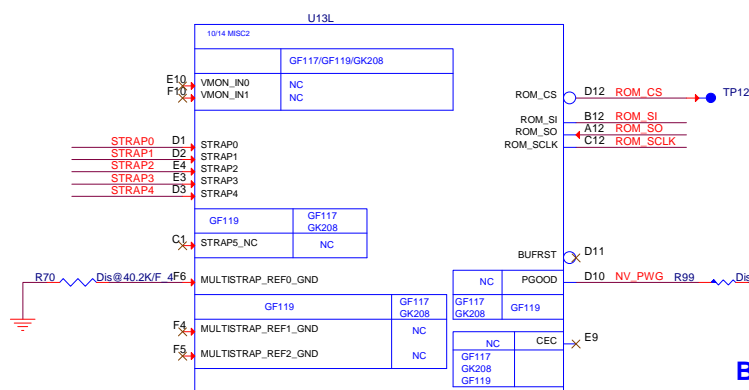
PEX IOVDD + PEX IOVDDQ = 1.042A

PEX\_PLL\_HVDD +  
PEX\_SVDD 3V3 = 143mA









4.99K: CS24992FB00 RES CHIP 4.99K 1/16W +1% (0402)  
45K: CS34502FB00 RES CHIP 45K 1/16W +1% (0402)  
15K: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)  
30.1K: CS33012FB18 RES CHIP 30.1K 1/16W +1% (0402)  
34.8K: CS33482FB22 RES CHIP 34.8K 1/16W +1% (0402)

## Binary Strap Mode Mapping

| Strap Pin name | Strap Mapping  | Resistance | Note   |
|----------------|--|------------|--|
| ROM_SCLK       | PCI_DEVID[4]<br>SUB_VENOR<br>PCI_DEVID[5]<br>PEX_PLL_EN        | 5Kohm , H  | 1000 , SUB: no Video BIOS  |
| ROM_SI         | RAM_CFG[2]<br>RAM_CFG[1]<br>RAM_CFG[0]                         | 5Kohm , H  | 4.99K 1000 --> Micron MT41K128M16JT-107G:K (Default)<br>30.1K 1101 --> Micron MT41K256M16HA-107G:E<br>34.8K 1110 --> Hynix H5TC4G63AFR-11C |
| ROM_SO         | FB[1]<br>FB[0]<br>SMB_ALT_ADDR<br>VGA_DEVICE                   | 5Kohm , H  | 1000 , FB: 256 MB (Default)<br>SMB:0x9E  |
| STRAP0         | User strap [3:0]   | 45Kohm , H | 1111 , EDID is used  |
| STRAP1         | 3GIO_CFG[3:0]  | 45Kohm , D | 1111 , USER defined  |
| STRAP2         | PCI_DEVID[3:0]   | 15Kohm , D | 010010 , N14P-GV2  |
| STRAP3         | SOR[3:0] EXPOSED   | 5Kohm , D  | 0000 , IFPx port not use   |
| STRAP4         | RESERVED<br>PCIE_SPEED_GEN3<br>PCIE_MAX_SPEED<br>DP_PLL_VDD33V | 45Kohm , D | 0111 , PCIE GEN3 setting   |

## GPIO ASSIGNMENTS ( GB2-64 )

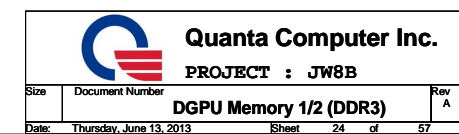
| GPIO  | I/O | PIN               | USAGE                         |
|-------|-----|-------------------|-------------------------------|
| 0     | IN  | FB_CLAMP_MON      | FB Clamp monitor              |
| 1     | OUT | MEM_VDD_CTL       | MEMORY VDD ID                 |
| 2     | OUT | LCD_BL_PWM        | LCD BACKLIGHT PWM             |
| 3     | OUT | LCD_VCC           | PANEL POWER ENABLE            |
| 4     | OUT | LCD_BLEN          | PANEL BACKLIGHT ENABLE        |
| 5     |     | RESERVE           |                               |
| 6     | OUT | FB_CLAMP_TGL_REQ# | # --> FB Clamp toggle request |
| 7     | OUT | 3Dvision          | 3D VISION LEFT/RIGHT VISION   |
| 8     | I/O | OVERT             | ACTIVE LOW THERMAL OVER TEMP  |
| 9     | I/O | ALERT             | ACTIVE LOW THERMAL ALERT      |
| 10    | OUT | MEM_VREF_CTL      | MEMORY VREF CONTROL           |
| 11    | OUT | PWM_VID           | GPU Core VDD PWM control      |
| 12    | IN  | PWR_LEVEL         | Power Detect ,HIGH=AC, LOW=DC |
| 13    | OUT | PSI               | Phase Shedding                |
| 14    | IN  | HPD_A             | HOT PLUG DETECT FOR IFPAB     |
| 15    | IN  | HPD_C             | HOT PLUG DETECT FOR IFPC      |
| 16    | OUT | FRM_LCK           | MEMMORY VDD CONTROL           |
| 17    | IN  | HPD_D             | HOT PLUG DETECT FOR IFPD      |
| 18    | IN  | HPD_E             | HOT PLUG DETECT FOR IFPE      |
| 19    | IN  | HPD_F or HPD_B    | HOT PLUG DETECT FOR IFPF      |
| 20/21 |     | RESERVE           |                               |

## VRAM Configuration Table

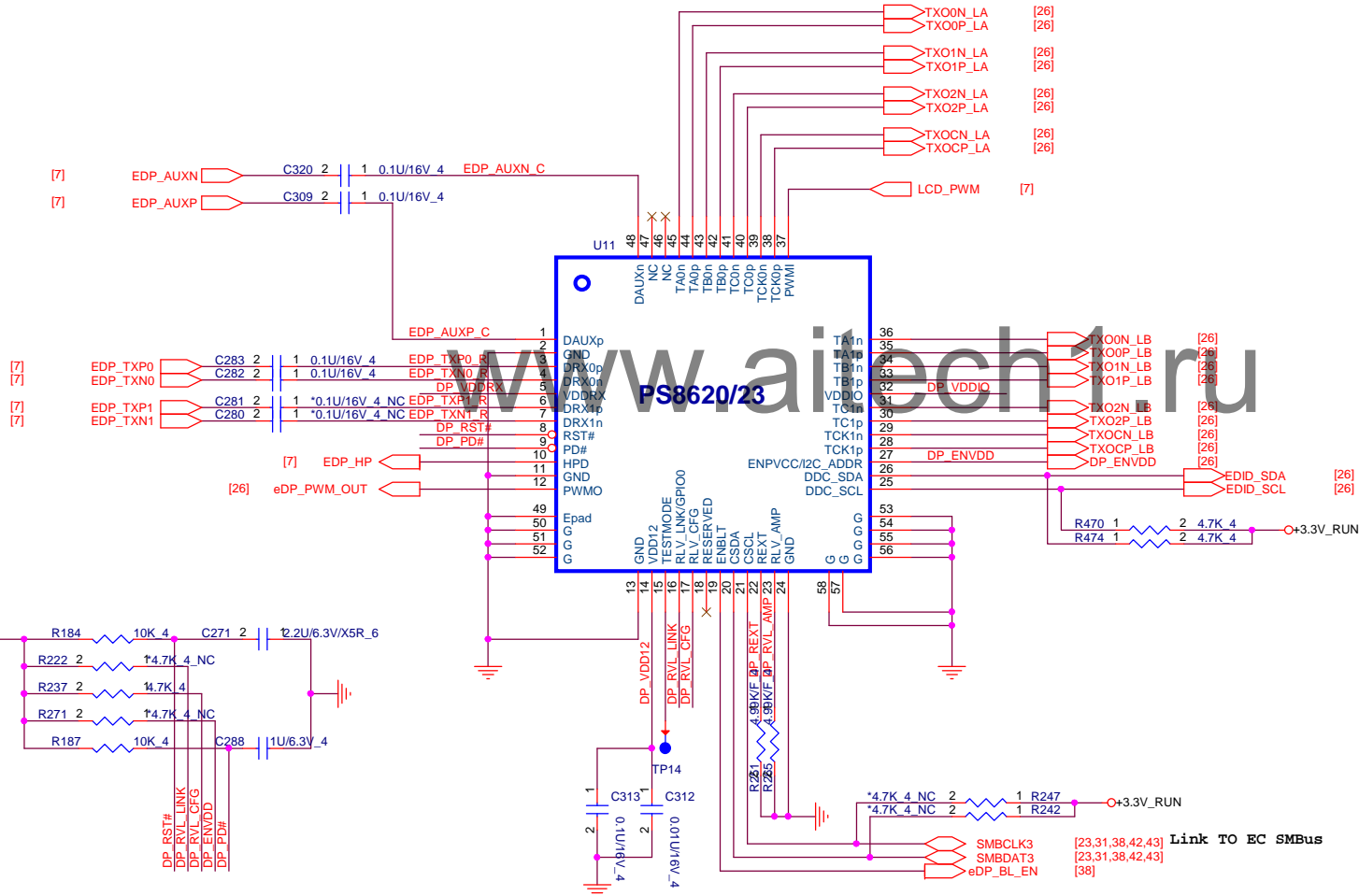
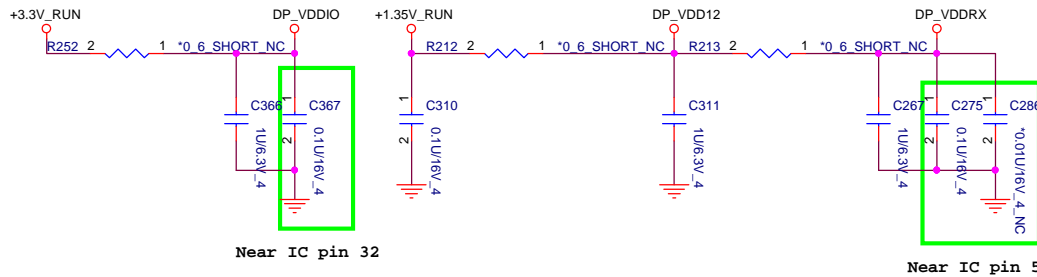
| RAMCFG [3:0] | DESCRIPTION                          | Vendor | DELL P/N | QC1 P/N     |
|--------------|--------------------------------------|--------|----------|-------------|
| 0000         |                                      |        |          |             |
| 1000<br>0x8  | MT41K128M16JT-107G:K<br>(FCBGA)(96P) | Micron | NA       | AKD5DGSTL00 |
| 1101<br>0xD  | MT41K256M16HA-107G:E                 | Micron | NA       | AKD5PGSTL00 |
| 1110<br>0xE  | H5TC4G63AFR-11C                      | Hynix  | NA       | AKD5PGWTW05 |

for meet Power down sequence for +3V\_GFX









DP\_ENVDD: I2C Slave address selection, internal pull-down ~80K  
 L: 0x10h-0x1Fh  
 H: 0x90h-0x9Fh

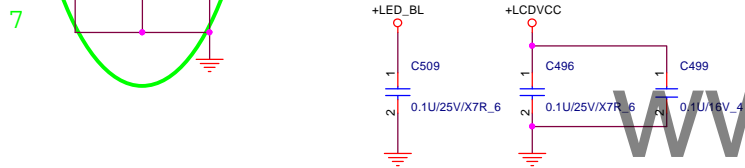
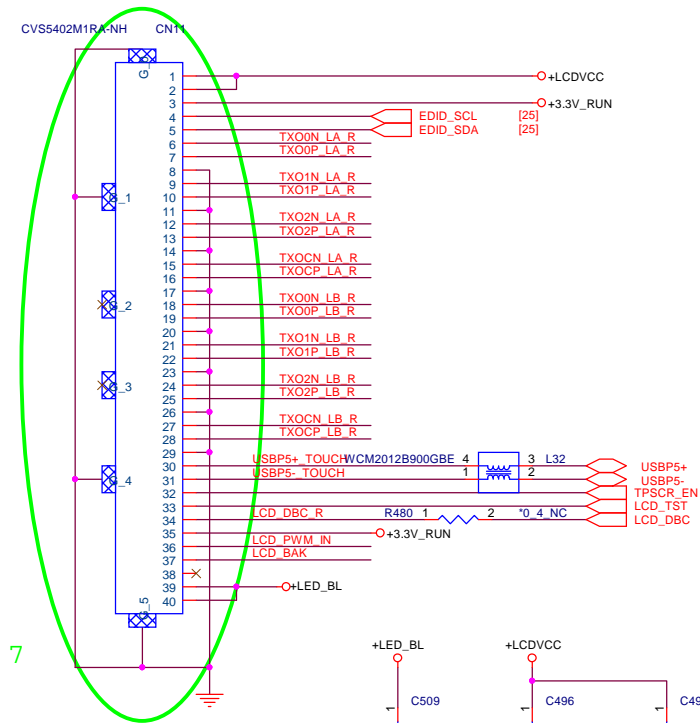
DP\_RVL\_LINK: LVDS single link or dual link selection, internal pull-down ~80K  
 L: Single link LVDS  
 H: Dual link LVDS



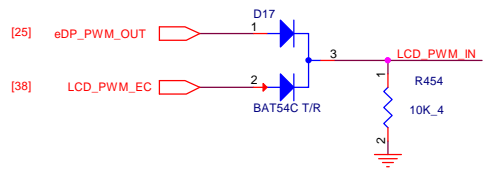
**Quanta Computer Inc.**

**PROJECT : JW8B**

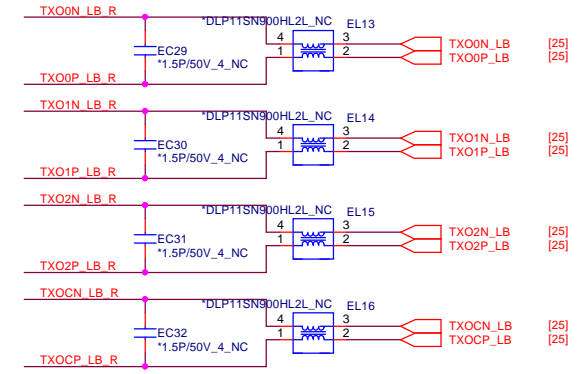
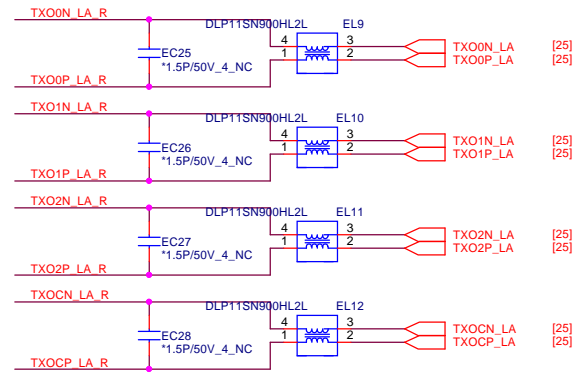
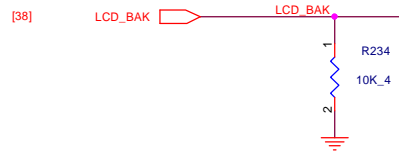
|       |                                |                |
|-------|--------------------------------|----------------|
| Size  | Document Number                | Rev A          |
|       | <b>eDP to LVDS (PS8620/23)</b> |                |
| Date: | Monday, July 08, 2013          | Sheet 25 of 57 |



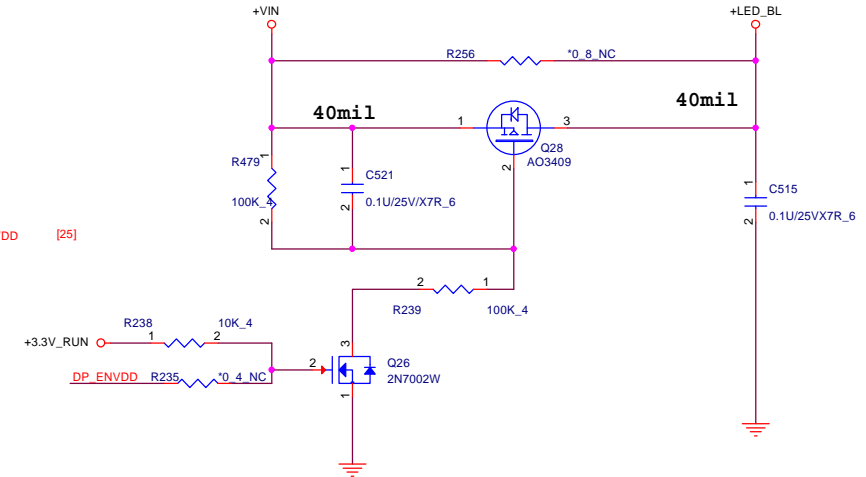
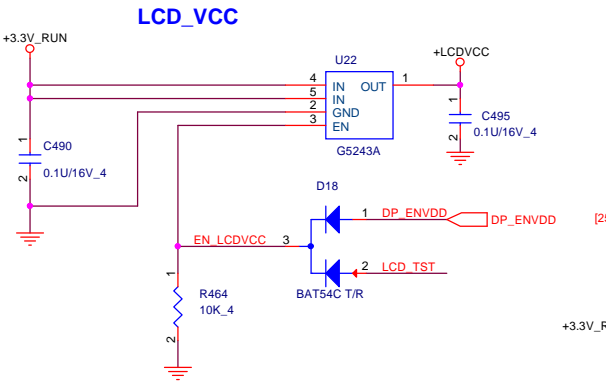
### Brightness Control



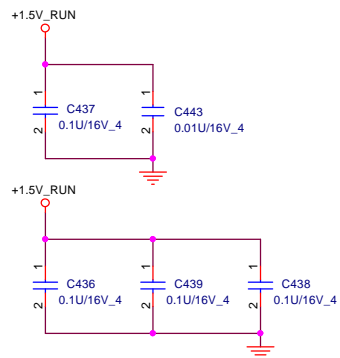
### BAK\_EN



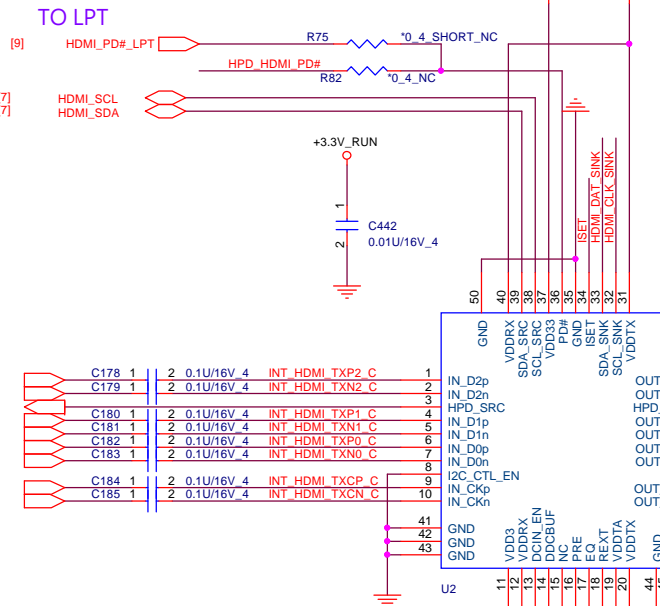
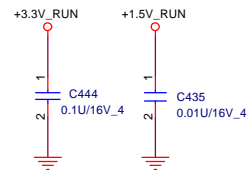
### TOUCH SCREEN



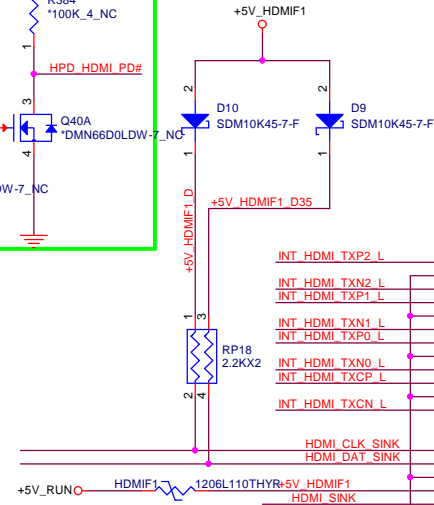
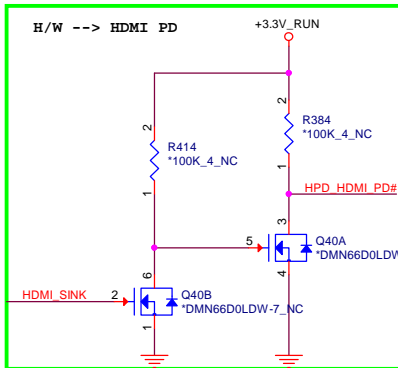
www.aitech1.ru



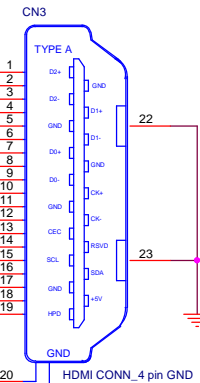
[7] INT\_HDMI\_TXP2  
[7] INT\_HDMI\_TXN2  
[7] INT\_HDMI\_HP  
[7] INT\_HDMI\_TXP1  
[7] INT\_HDMI\_TXN1  
[7] INT\_HDMI\_TXP0  
[7] INT\_HDMI\_TXN0  
[7] INT\_HDMI\_TXCP  
[7] INT\_HDMI\_TXCN



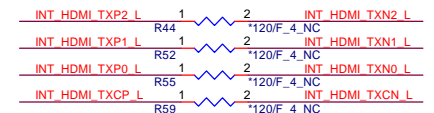
www.aitech1.ru



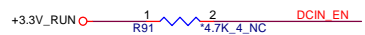
HDMI CN



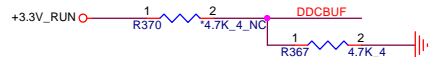
EMI



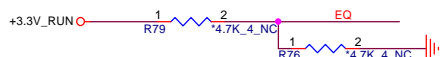
3 Level Input:  
L:LOW,internal pull down  
H:HIGH, external pull up  
M:VDD3/2, both external pill-up and pull-down



Int pull-down 150k , 3.3V IO  
L:default,AC coupling input  
H:DC coupling input



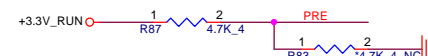
L:default,passive DDC pass-through  
H:active DDC buffer with default threshold  
M:passive DDC pass-through with internal ~10Kohm pull up



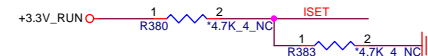
L:programmable EQ for channel loss up to 6.5dB @3Gbps  
H:programmable EQ for channel loss up to 9.5dB @3Gbps  
M:programmable EQ for channel loss up to 3dB @3Gbps



Int pull-down 150k , 3.3V IO  
L:HDMI ID disable  
H:HDMI ID enable



L:no pre-emphasis  
H:1.6dB pre-emphasis  
M:3.0dB pre-emphasis



L:default  
H:increase +13%  
M:increase -13%



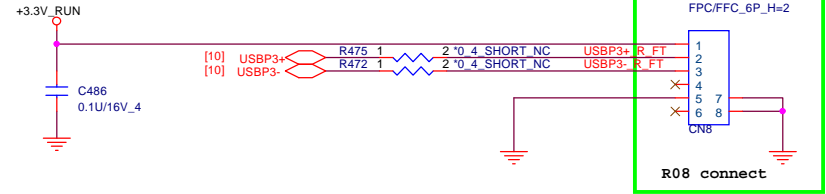
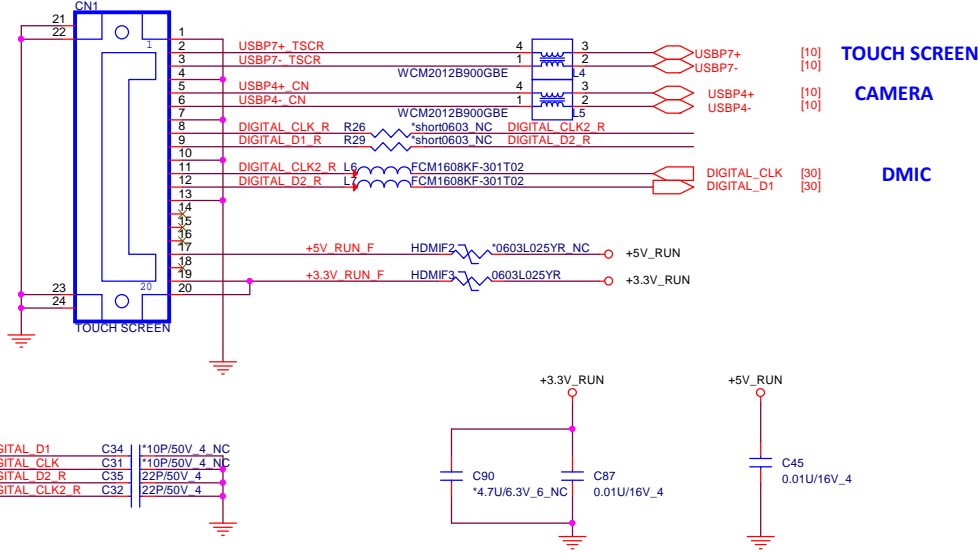
Quanta Computer Inc.

PROJECT : JW8B

# CAMERA / DMIC

# Fingerprint

Conn P/N, Footprint OK. Luke 12/18



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Quanta Computer Inc.

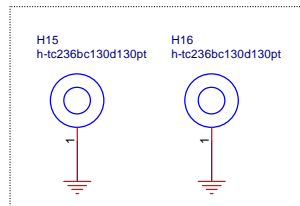
PROJECT : JW8B

|      |                       |                |
|------|-----------------------|----------------|
| Size | Document Number       | Rev A          |
| Date | Monday, July 08, 2013 | Sheet 28 of 57 |

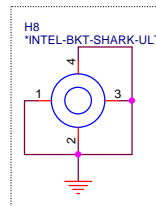
Camera/Fingerprint Conn

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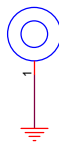
### Mini-PCIE



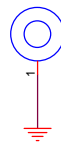
### CPU BKT



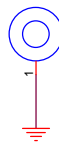
H7  
\*H-TC394BC315D130P2



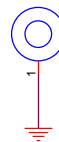
H10  
\*h-tc394bc315d138p2



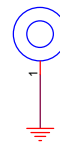
H11  
\*h-tc394bc315d138p2



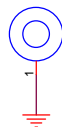
H13  
\*h-tc394bc315d138p2



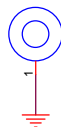
H14  
\*h-tc276bc315d118p2



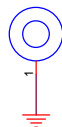
H3  
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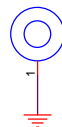
H4  
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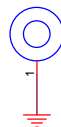
H6  
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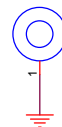
H12  
\*h-tc236bc315d98p2



H5  
\*h-tc315bc150d150pt



H9  
\*h-tc315i190bc150d150pt



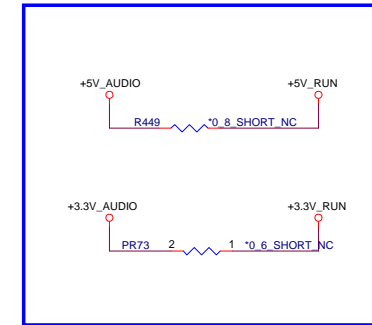
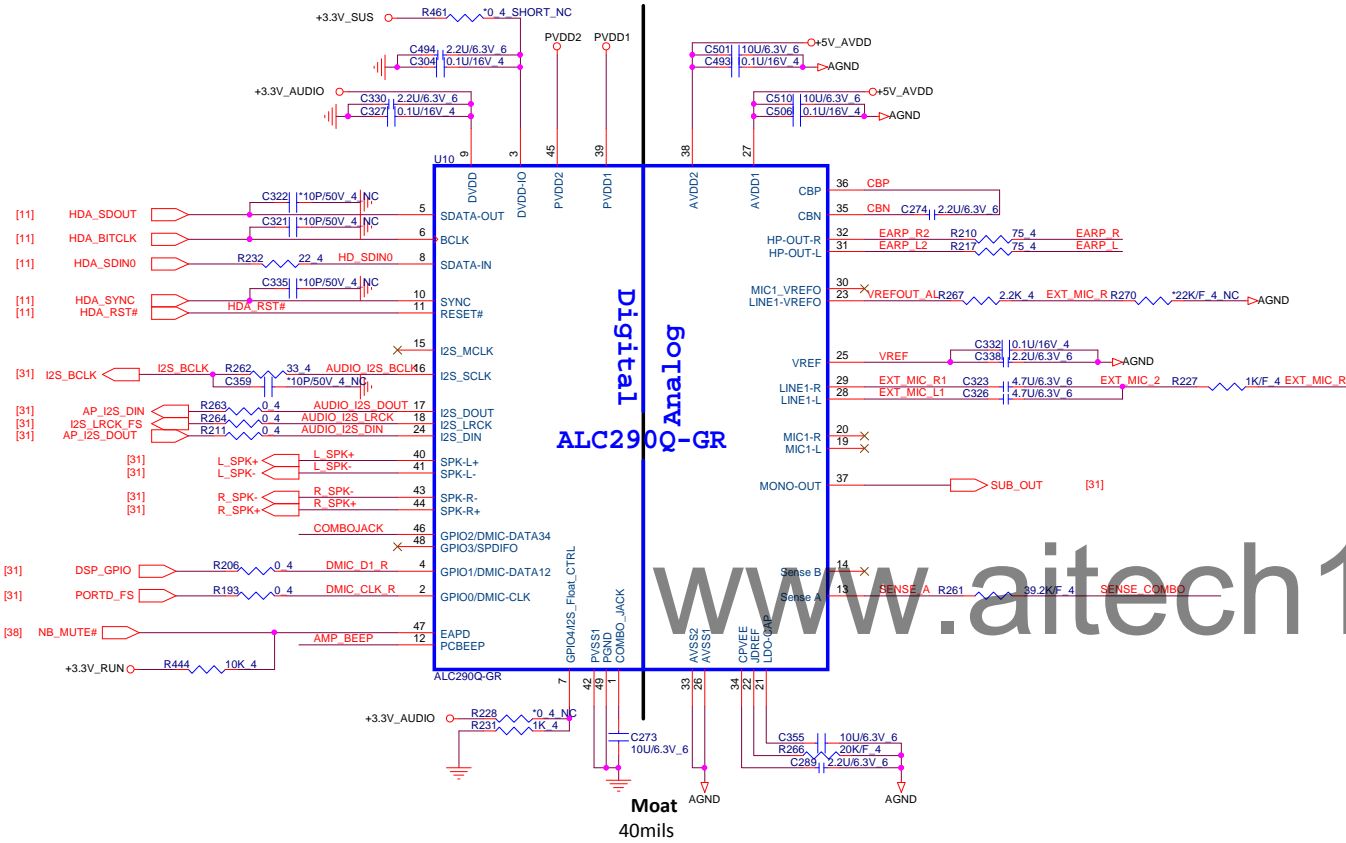
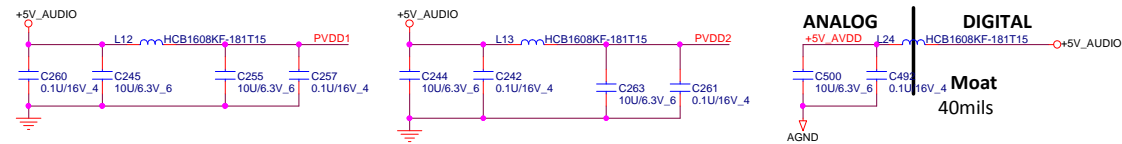
H1  
\*h-c59d59n



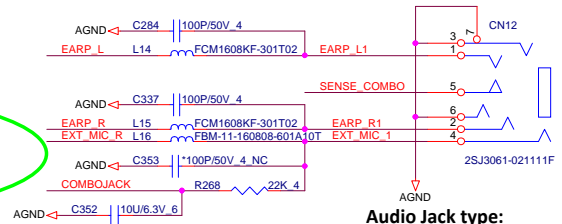
H2  
\*h-c59d59n



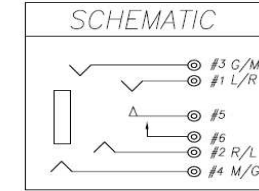
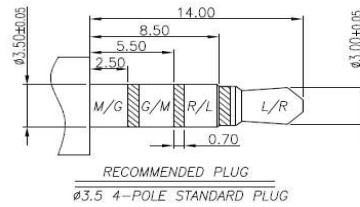
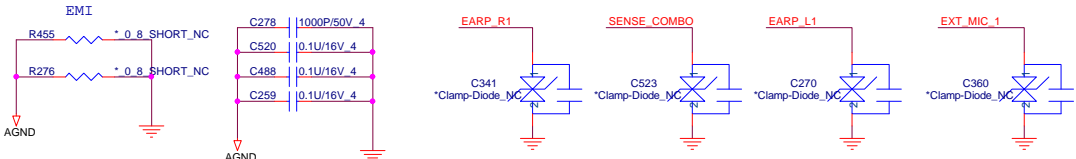
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|---------|----------------------|-------|----------|
| Title   |                      |       |          |
| <Title> |                      |       |          |
| Size    | Document Number      |       |          |
| Custom  | <Doc>                |       |          |
| Date:   | Friday, May 10, 2013 | Sheet | 29 of 57 |
|         |                      |       | Rev A    |



## Audio Combo Jack



Audio Jack type:  
Normal Open  
Combo Jack(IPHONE)





VDD10

C483 0.1U/16V 4

C480 0.1U/16V 4

C479 0.1U/16V 4

C482 0.1U/16V 4

[illegible]

|     |               |      |            |             |    |          |
|-----|---------------|------|------------|-------------|----|----------|
|     | PCIE_TXP3     | C210 | 0.1U/16V 4 | PCIE_TXP3_C | 13 | CREG0    |
| [0] | PCIE_TXN3     | C213 | 0.1U/16V 4 | PCIE_TXN3_C | 14 | HSIN     |
| [2] | CLK_PCIE_LANP |      |            |             | 15 | REFCLK_P |
|     | CLK_PCIE_LANN |      |            |             | 16 | REFCLK_N |

|      |           |      |            |             |  |  |
|------|-----------|------|------------|-------------|--|--|
| [10] | PCIE_RXP3 | C214 | 0.1U/16V 4 | PCIE_RXP3_C |  |  |
| [10] | PCIE_RXN3 | C216 | 0.1U/16V 4 | PCIE_RXN3_C |  |  |

[13,20,33,37] PLTRST#

+3VLANVCC

R431 10K 4 NC

R433 1 2 10 4 SHORT NC

LAN\_RST#

+3.3V\_RUN

1K 4

R435

LAN\_ISOLAT#

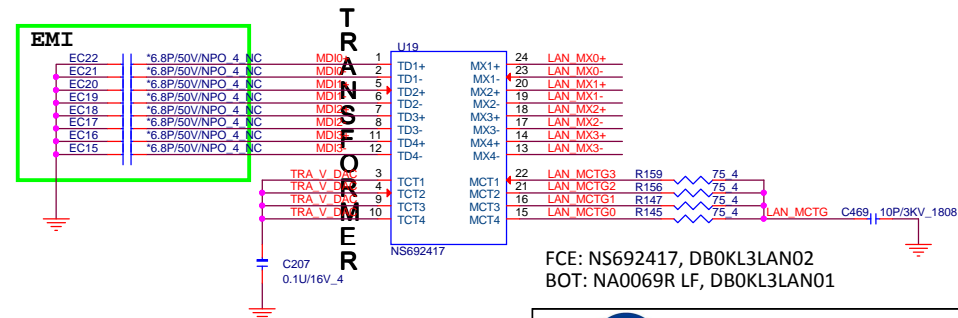
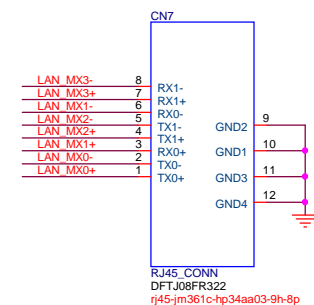
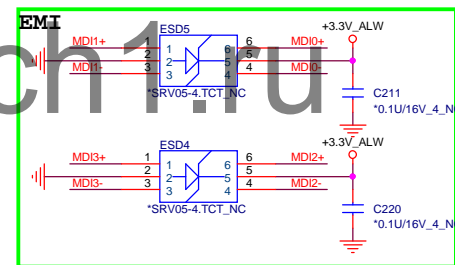
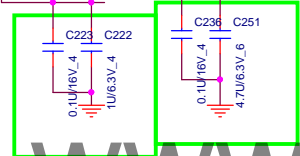
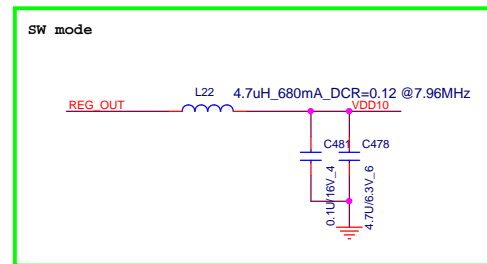
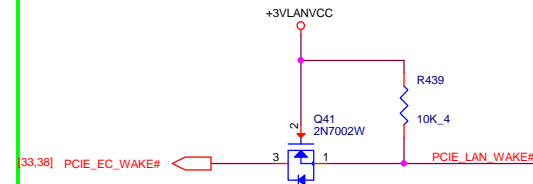
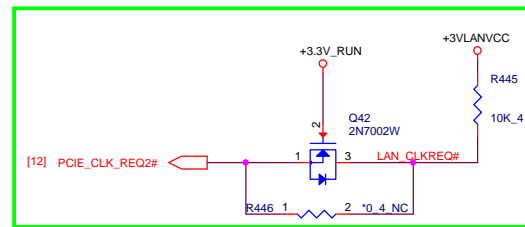
\*15K 4 NC

R436

The schematic diagram illustrates the pin configuration for the LAN\_PWR\_EN\_EC pin. The central component is the PUI2 TPS22965DSGR. The connections are as follows:

- VIN\_O1** (Pin 1) is connected to +3.3V\_ALW through capacitor PC38 (1uF/6.3V\_4).
- VIN\_O2** (Pin 2) is connected to +3.3V\_ALW.
- VOUT\_O1** (Pin 7) is connected to +3.3V\_ALW through resistor R174 (0.6 SHORT NC).
- VOUT\_O2** (Pin 8) is connected to +3.3V\_ALW through resistor R453 (0.6 SHORT NC).
- ON** (Pin 6) is connected to +5V\_ALW through resistor PR61 (0.4 SHORT NC).
- CT** (Pin 3) is connected to +5V\_ALW through capacitor PC43 (0.1uF/25V\_4).
- VBIAS** (Pin 4) is connected to +5V\_ALW through capacitor PC39 (0.01uF/16V\_4).
- PAQ** (Pin 9) is connected to +5V\_ALW through capacitor PC167 (0.1uF/25V\_4).
- GND** (Pin 5) is connected to ground through capacitor PC42 (1000P/50V\_4).

The diagram also shows the connection of the LAN\_PWR\_EN\_EC pin to the +3.3V\_RUN power source through a resistor R453 (0.6 SHORT NC).



FCE: NS692417, DB0KL3LAN02  
BOT: NA0069R LF, DB0KL3LAN01



PROJECT : JW8B

|       |                             |                |
|-------|-----------------------------|----------------|
| Size  | Document Number             | Rev            |
|       | <b>LAN(RTL8111GUS)/RJ45</b> | <b>A</b>       |
| Date: | Monday, July 08, 2013       | Sheet 32 of 57 |





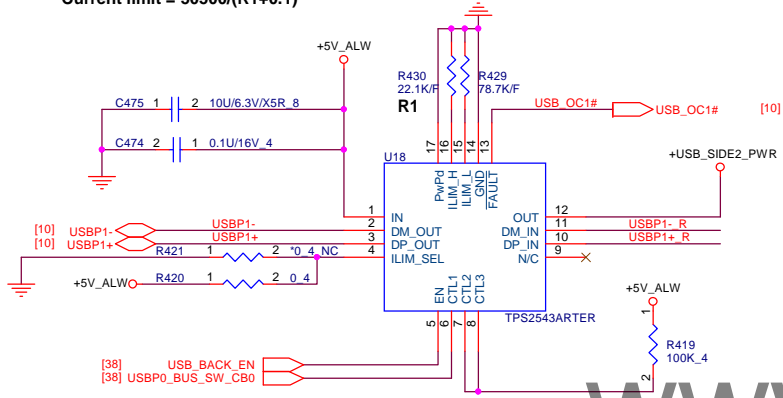
USB3.0 Power Share

USB Power share

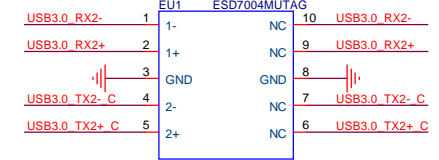
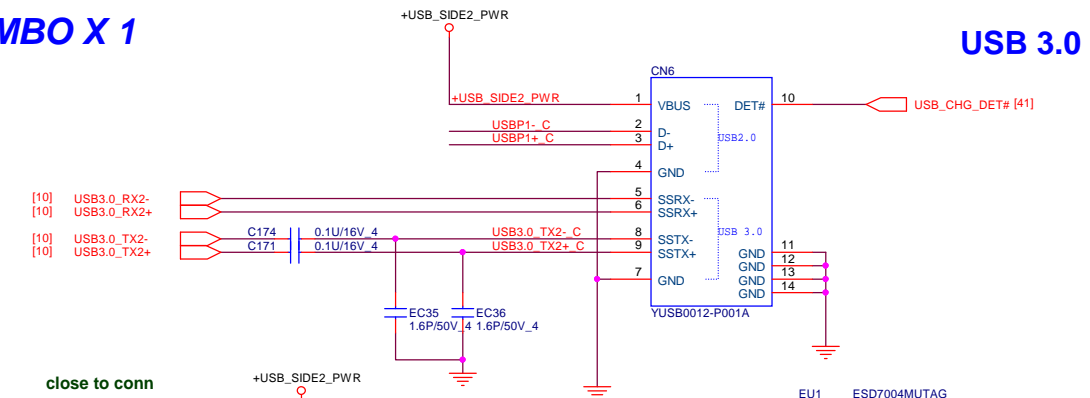
| USBP0_BUS_SW_CB0 |           | Mode             |
|------------------|-----------|------------------|
| Low              |           | DCP, Auto-detect |
| High             |           | CDP, BC Spec 1.2 |
| OC limitation    | R1        | mA               |
|                  | 100k ohm  | 504              |
|                  | 22.1k ohm | 2274             |

Applied Now

Current limit = 50500/(R1+0.1)

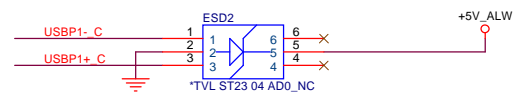


USB3.0/2.0 COMBO X 1



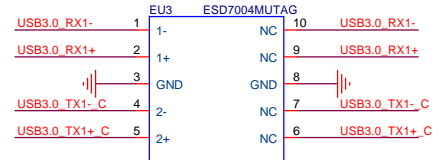
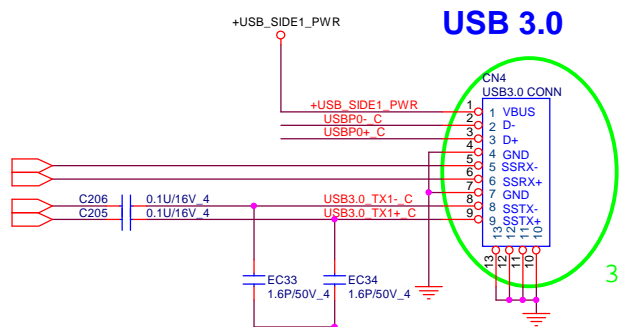
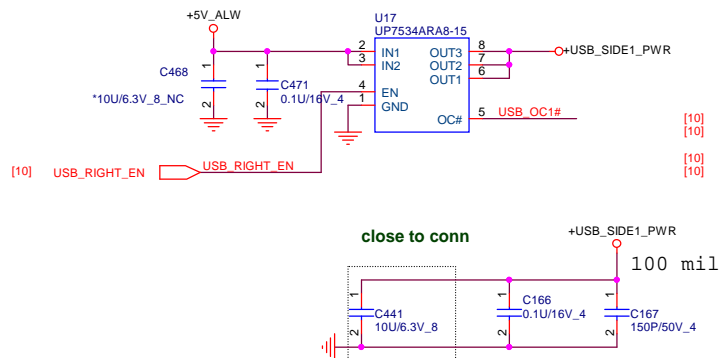
ESD Function

Place ESD diodes as close as USB connector.



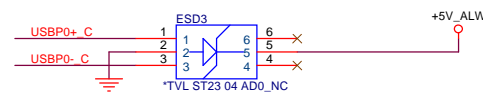
USB3.0/2.0 COMBO

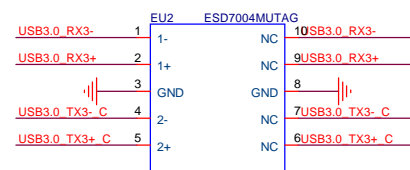
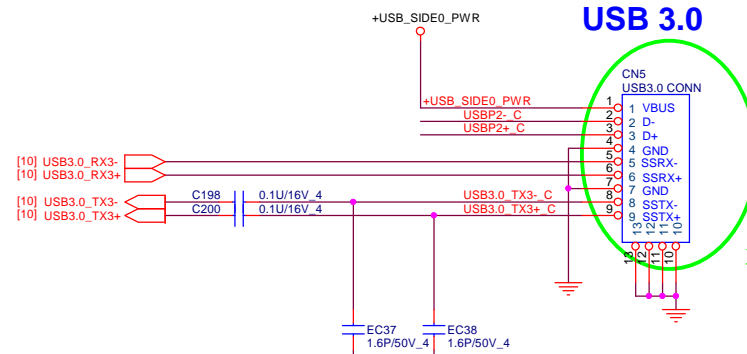
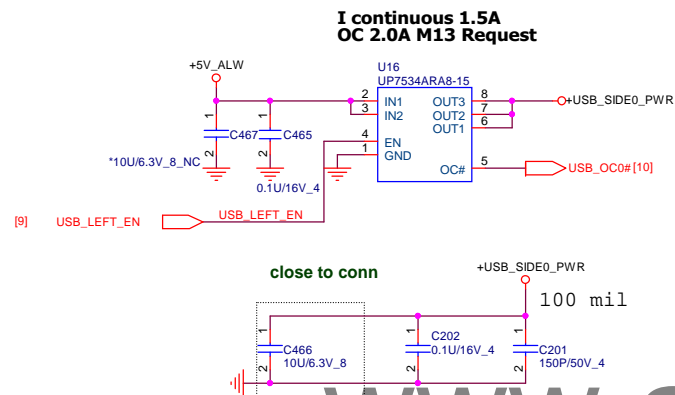
I continuous 1.5A  
OC 2.0A M13 Request



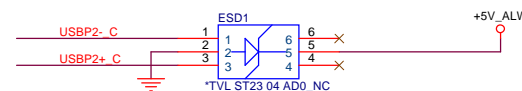
ESD Function

Place ESD diodes as close as USB connector.



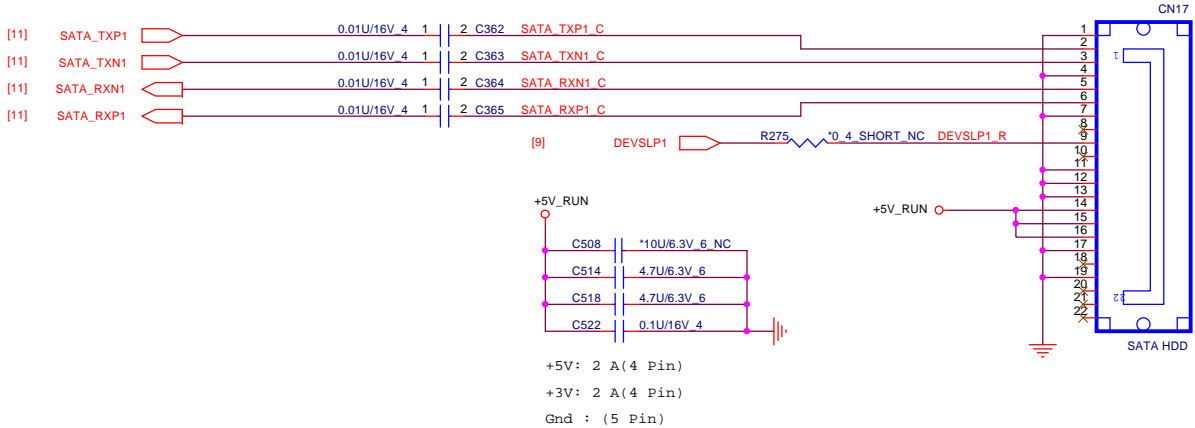


**ESD Function**  
Place ESD diodes as close as USB connector.



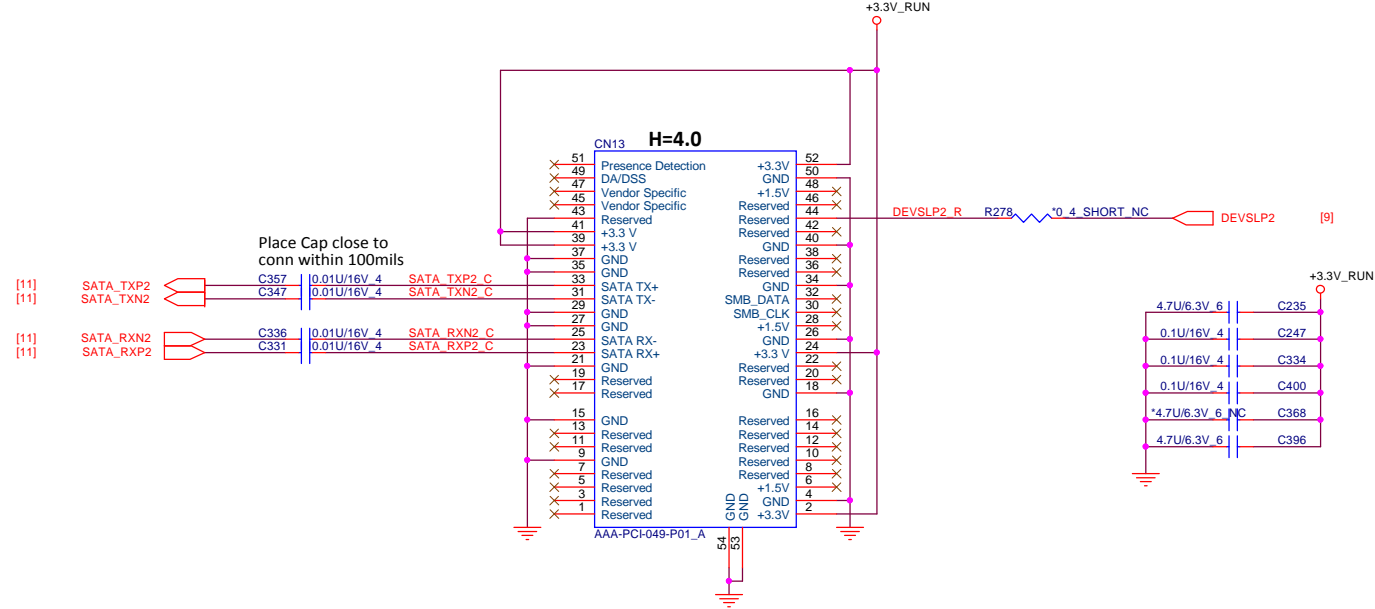
**Quanta Computer Inc.**  
**PROJECT : JW8B**

SATA HDD Connector

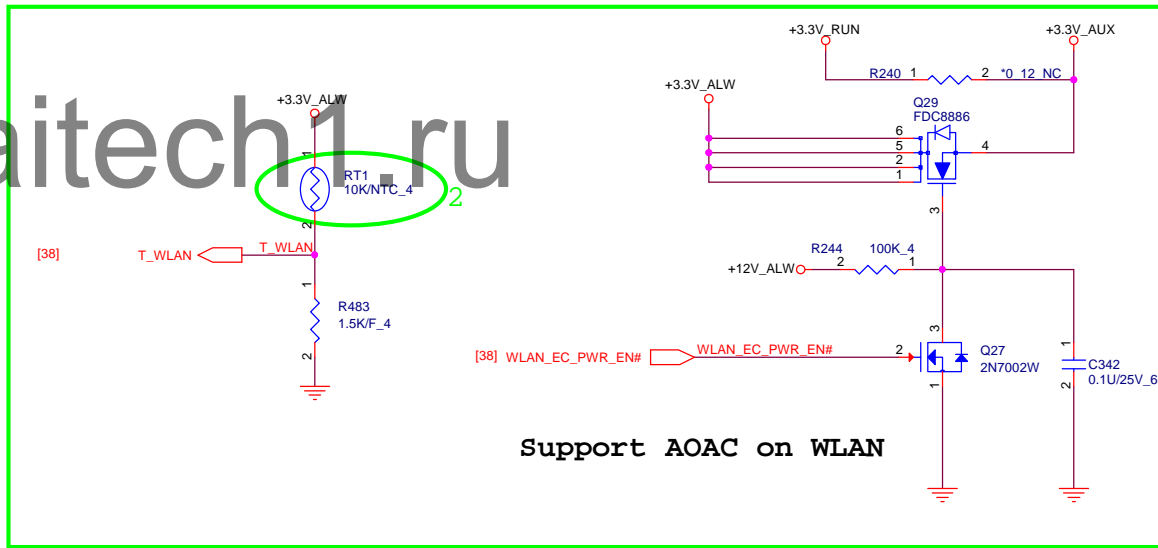
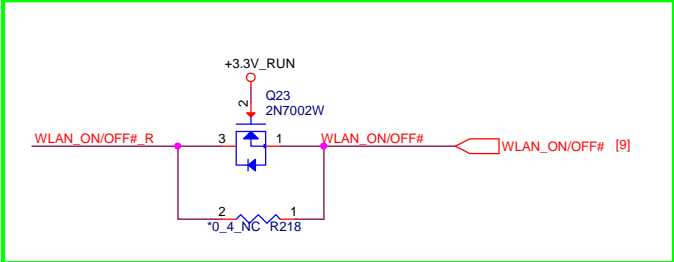
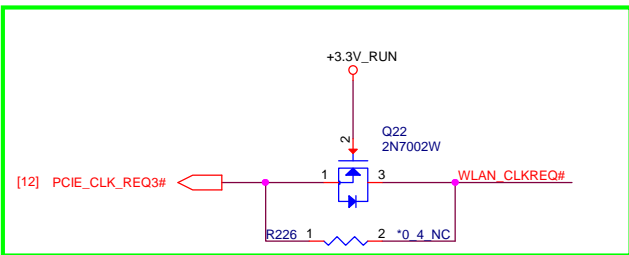
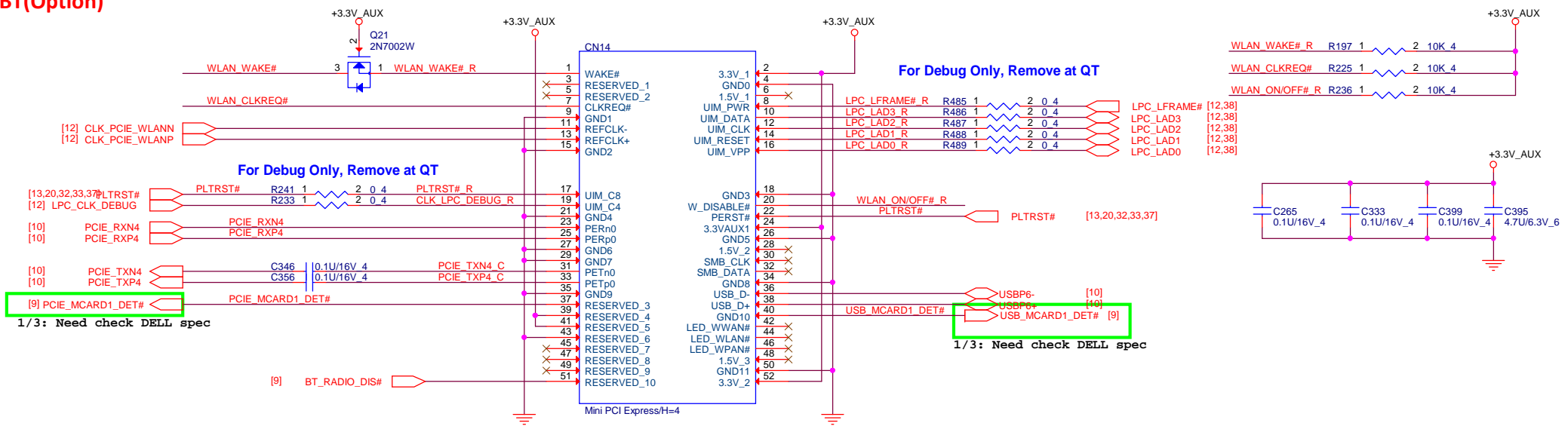


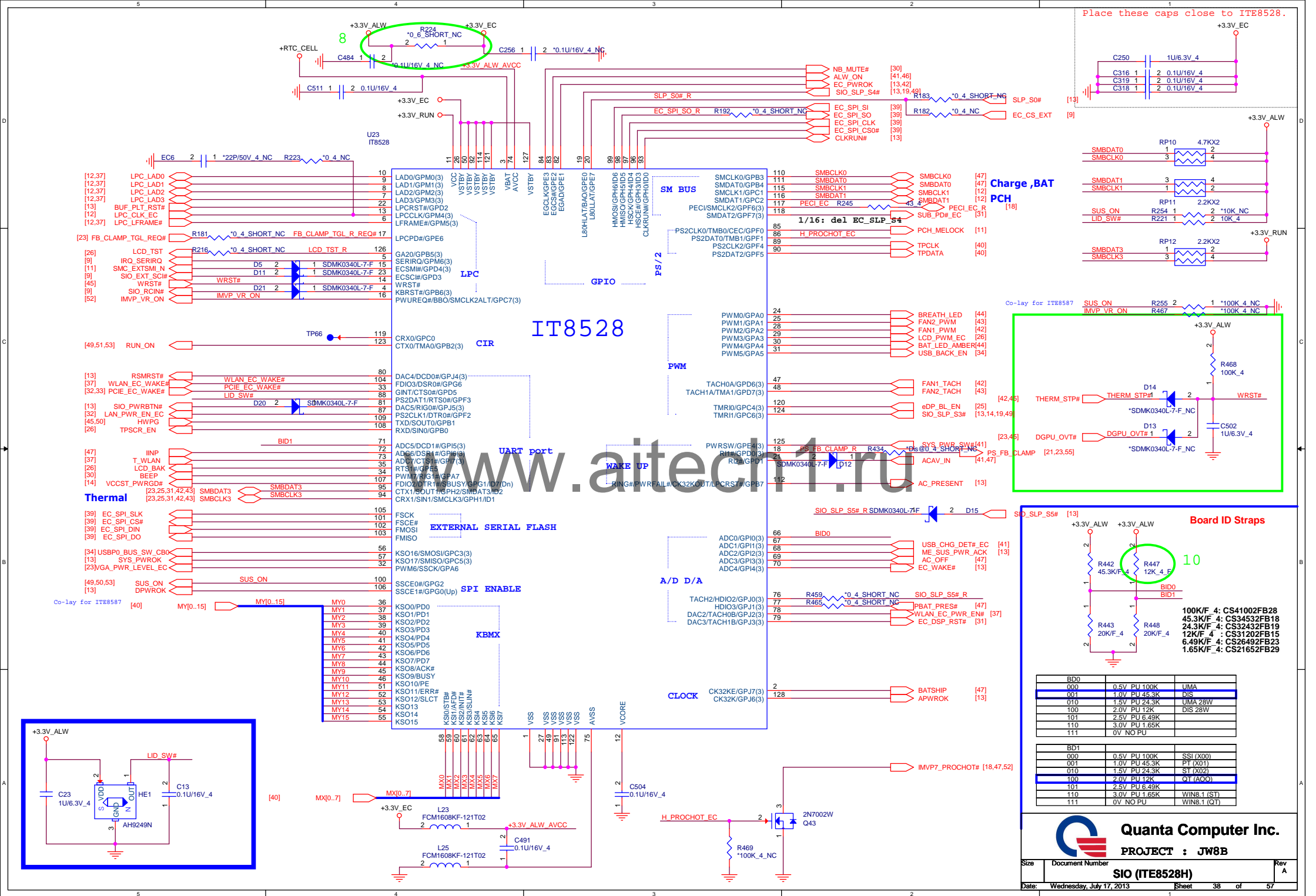
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mSATA

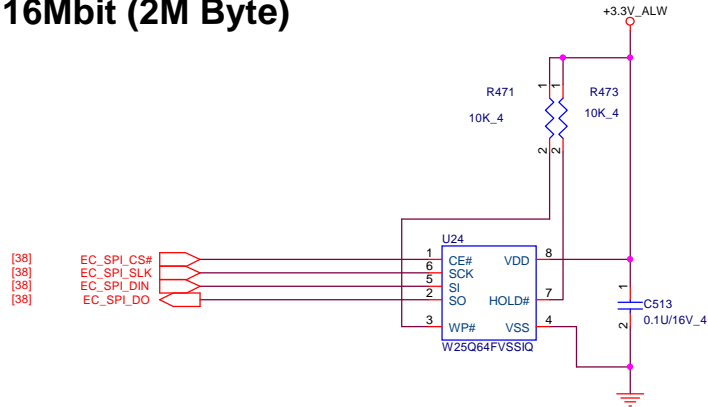


# Mini Card WLAN/BT(Optional)

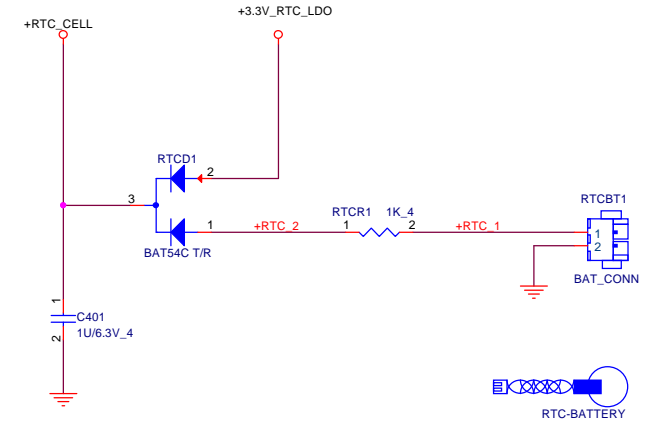




## For EC 16Mbit (2M Byte)

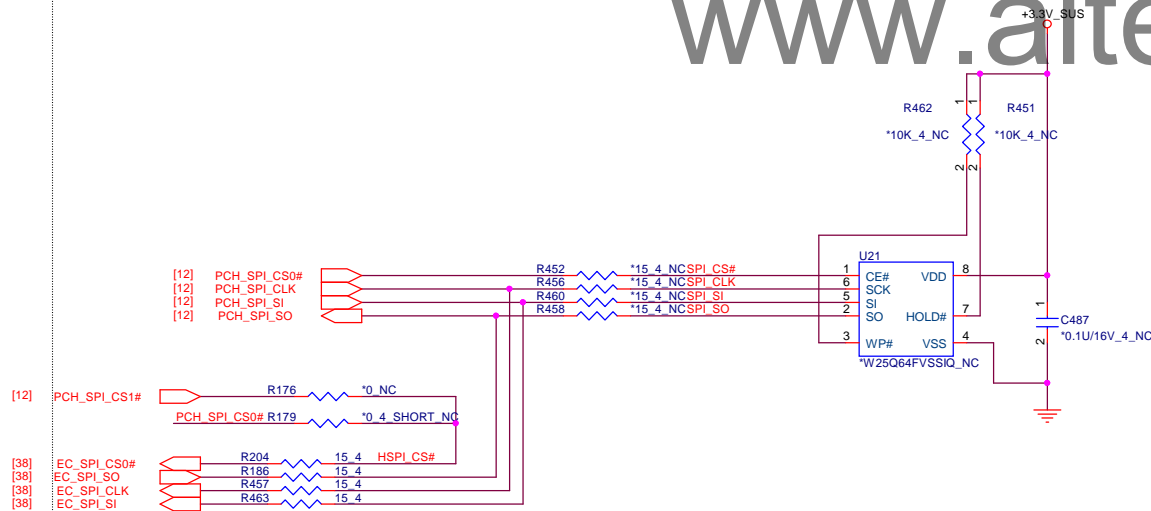


## RTC BATTERY



## For PCH 64Mbit (8M Byte)

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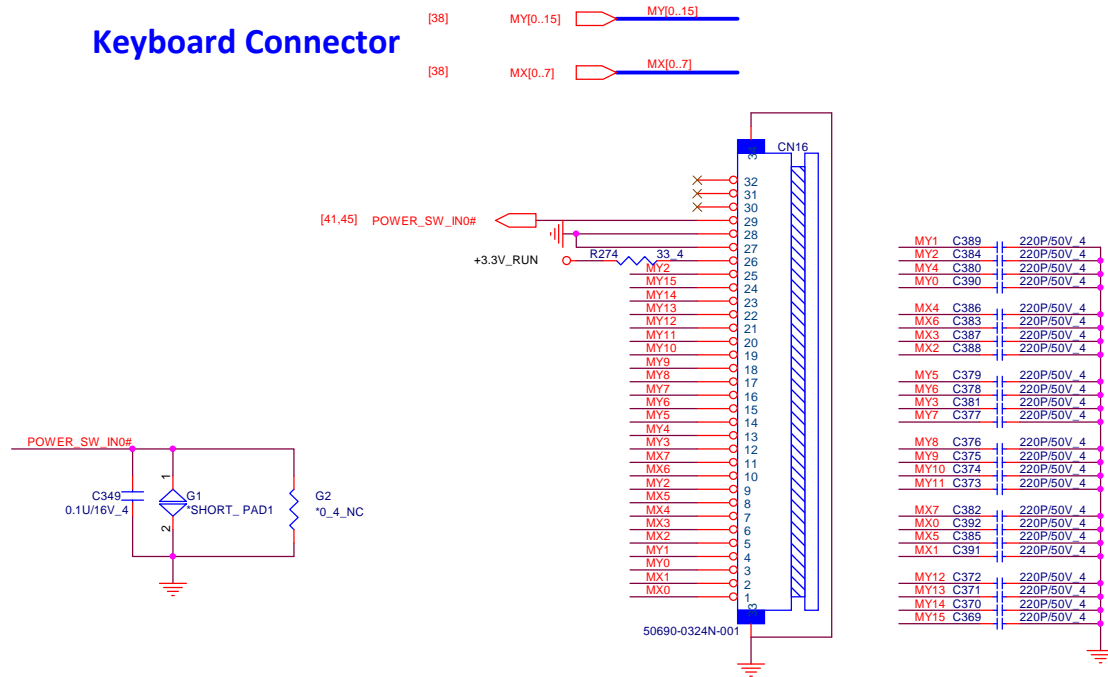


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PROJECT : JW8B

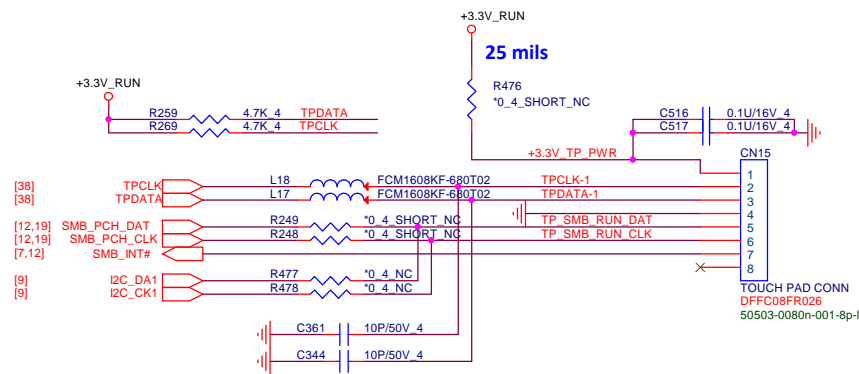
| Size        | Document Number       | Rev            |
|-------------|-----------------------|----------------|
|             |                       | A              |
| FLASH / RTC |                       |                |
| Date:       | Monday, July 08, 2013 | Sheet 39 of 57 |

## Keyboard Connector



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## Touch Pad Connector



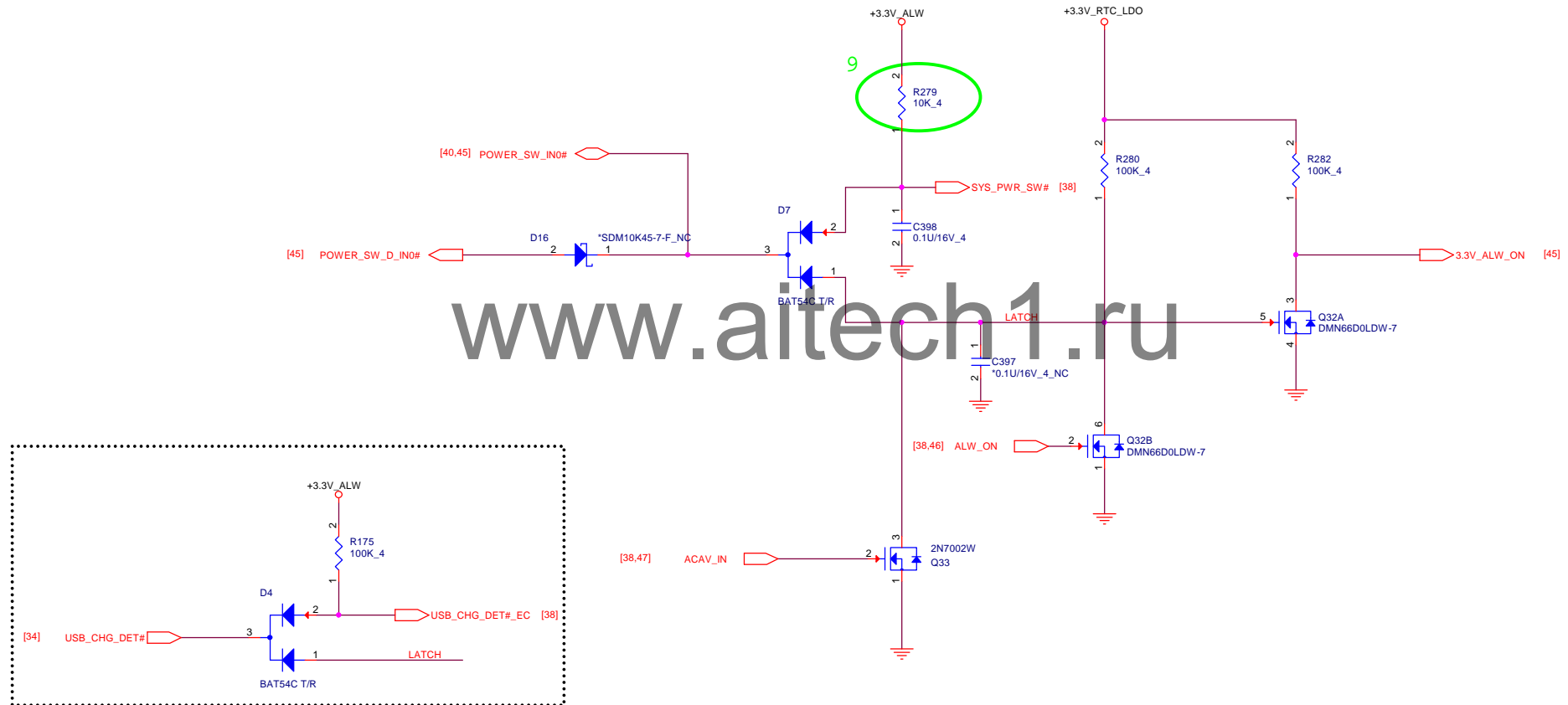
Quanta Computer Inc.

PROJECT : JW8B

KB/CLK Gen/FAN/TP



## 3VALW ON POWER LOGIC



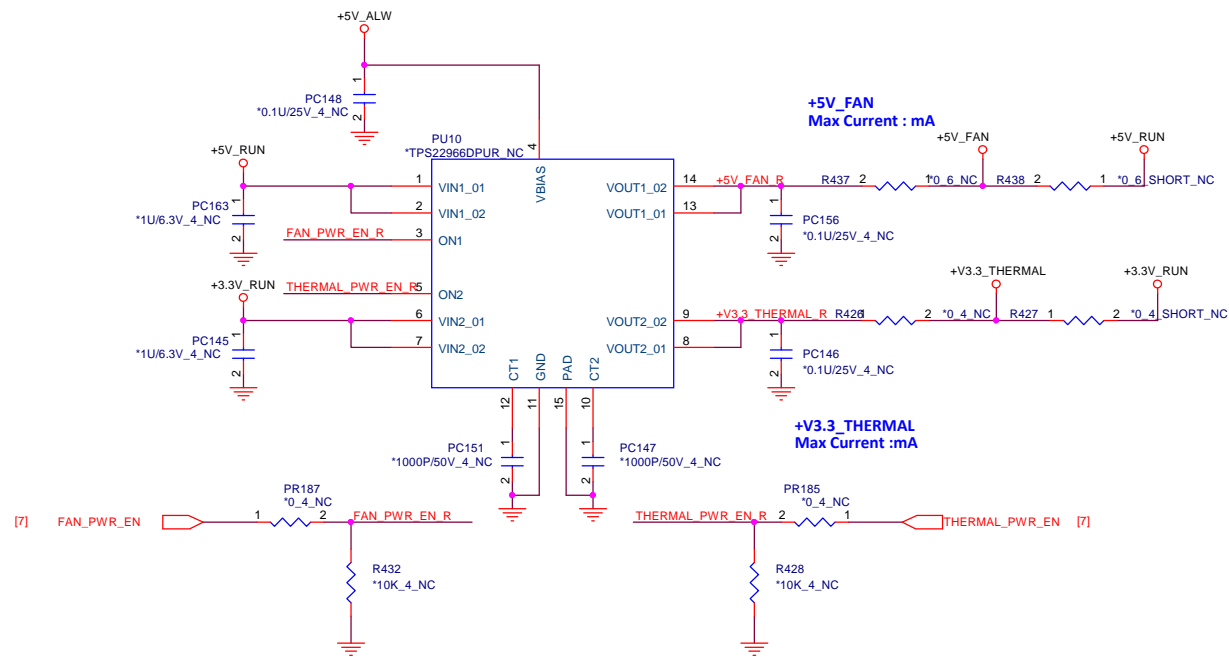
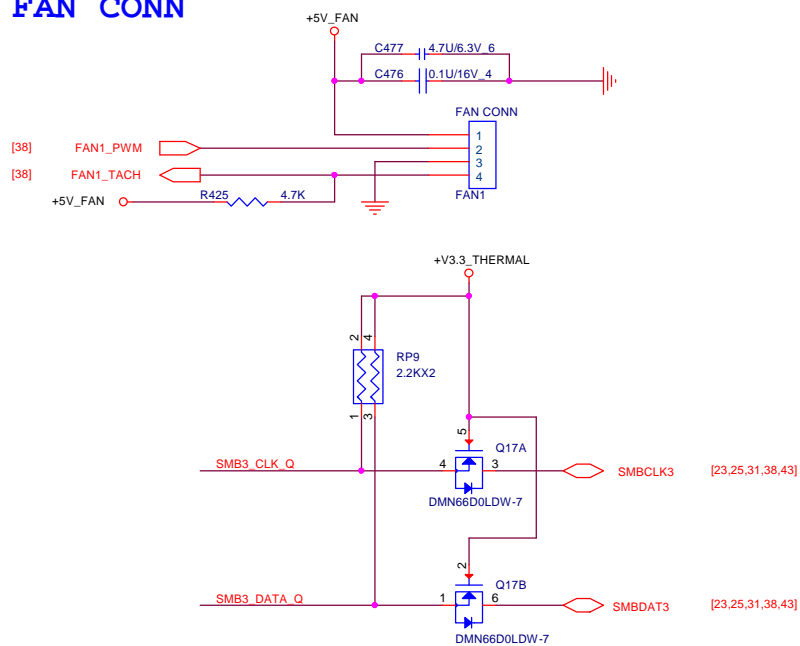
**Quanta Computer Inc.**

**PROJECT : JW8B**

**3VALW ON POWER LOGIC**

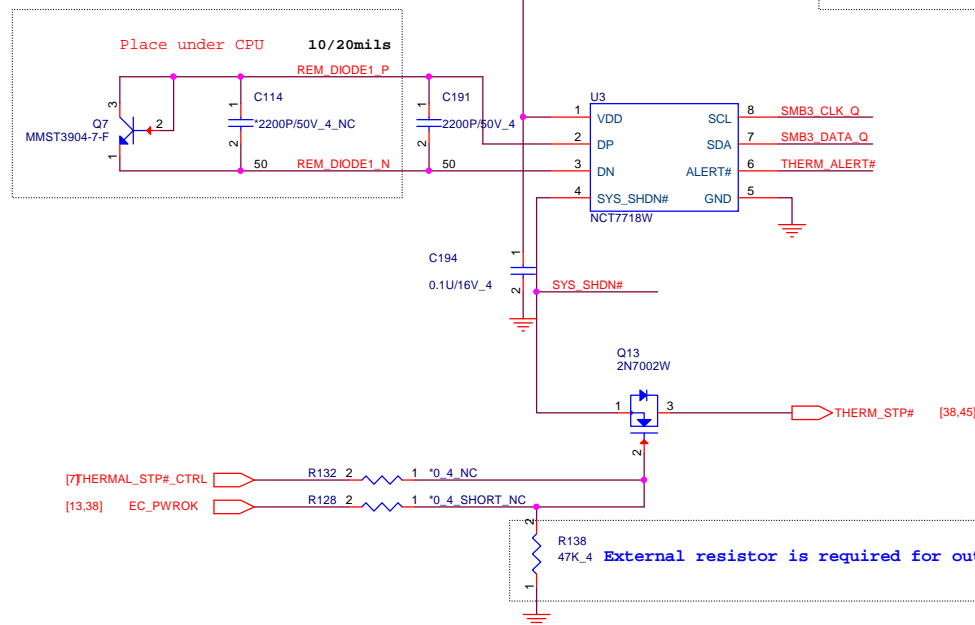
|                                |                 |     |
|--------------------------------|-----------------|-----|
| Size                           | Document Number | Rev |
| Date: Wednesday, July 17, 2013 | Sheet 41 of 57  | A   |

## FAN CONN



## THERMAL IC

Need closed to CPU



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OTP 91 degree C

OTP 85 degree : R139= 18.7K, R115 = 2K

| SYS_SHDN# | 2K   | 7.5K | 10.5K | 14K   | 18.7K |
|-----------|------|------|-------|-------|-------|
| ALERT#    |      |      |       |       |       |
| 2K        | 77'C | 87'C | 97'C  | 107'C | 117'C |
| 7.5K      | 79'C | 89'C | 99'C  | 109'C | 119'C |
| 10.5K     | 81'C | 91'C | 101'C | 111'C | 121'C |
| 14K       | 83'C | 93'C | 103'C | 113'C | 123'C |
| 18.7K     | 85'C | 95'C | 105'C | 115'C | 125'C |

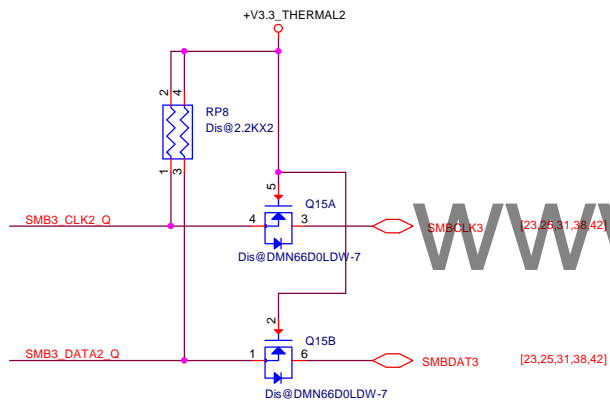
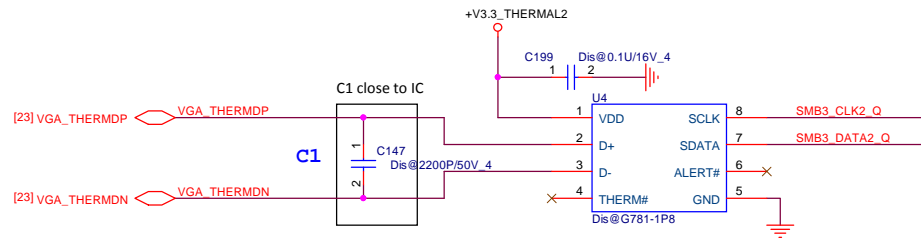


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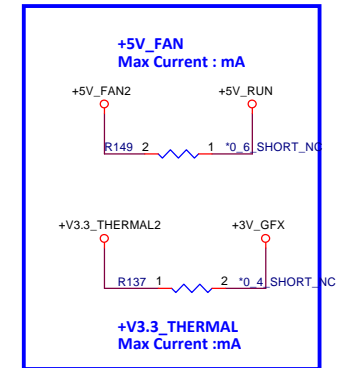
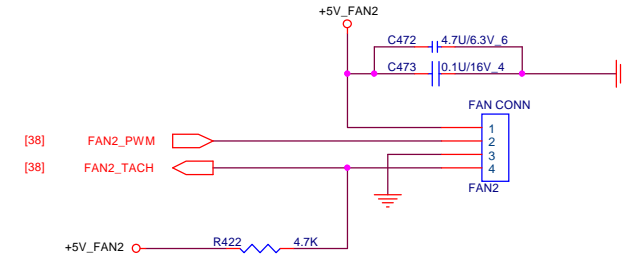
PROJECT : JW8B

## For GPU use

G781-1P8  
SMBus address is 1001101xb (9Ah) (x is R/W bit).



## FAN CONN



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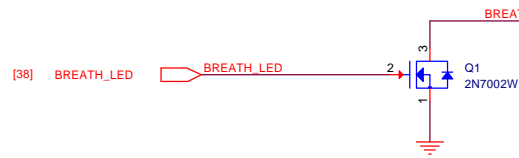


Quanta Computer Inc.

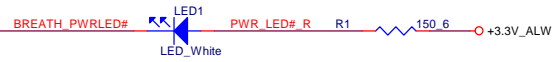
PROJECT : JW8B

| Size  | Document Number       | Rev            |
|-------|-----------------------|----------------|
|       | Thermal GPU           | A              |
| Date: | Monday, July 08, 2013 | Sheet 43 of 57 |

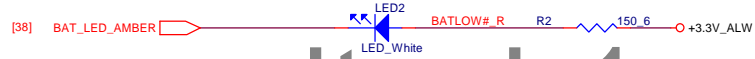
### LED Status



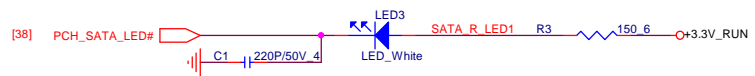
### System status LED



### Battrey charger LED



### HDD access LED



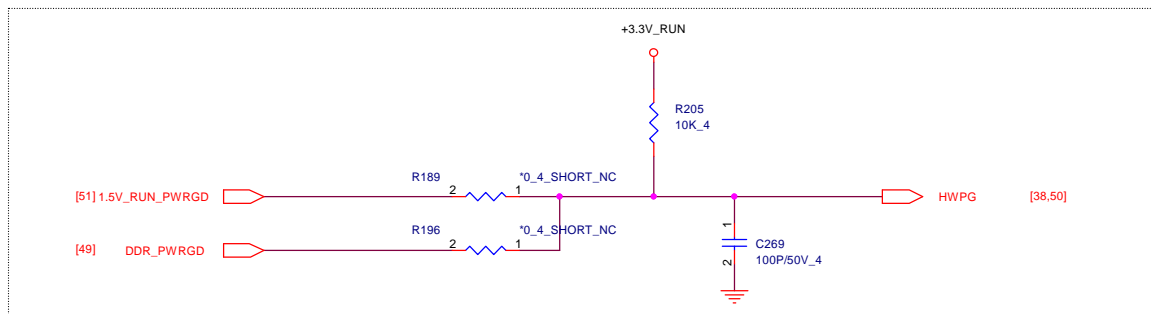
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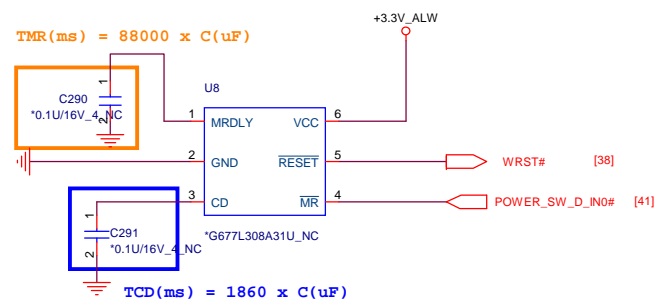
Quanta Computer Inc.

PROJECT : JW8B

|       |                      |                |
|-------|----------------------|----------------|
| Size  | Document Number      | Rev            |
|       | LED                  | A              |
| Date: | Friday, May 10, 2013 | Sheet 44 of 57 |



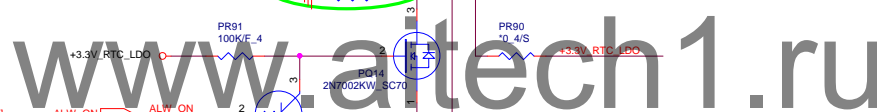
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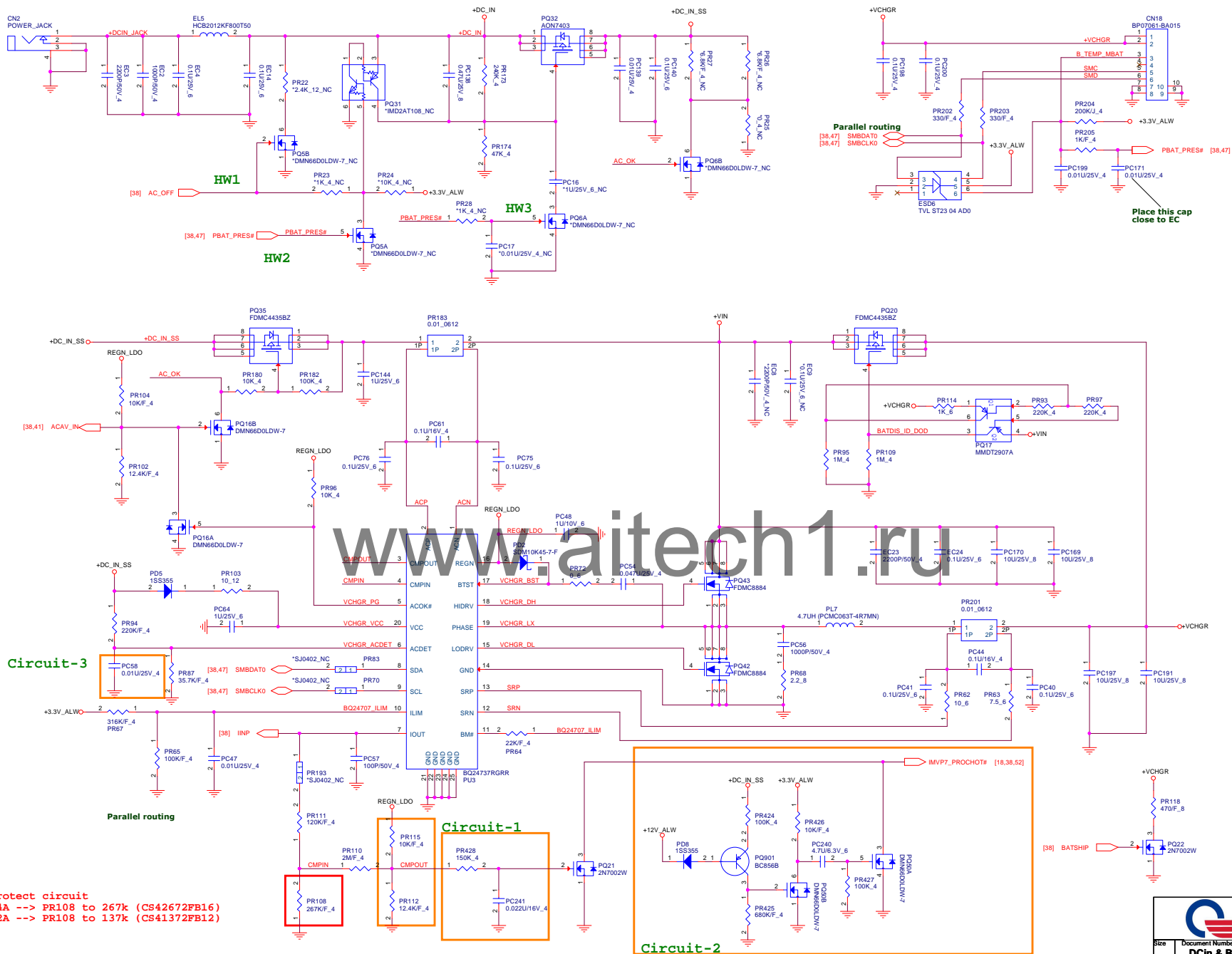


Quanta Computer Inc.


PROJECT : JW8B

System Reset Circuit



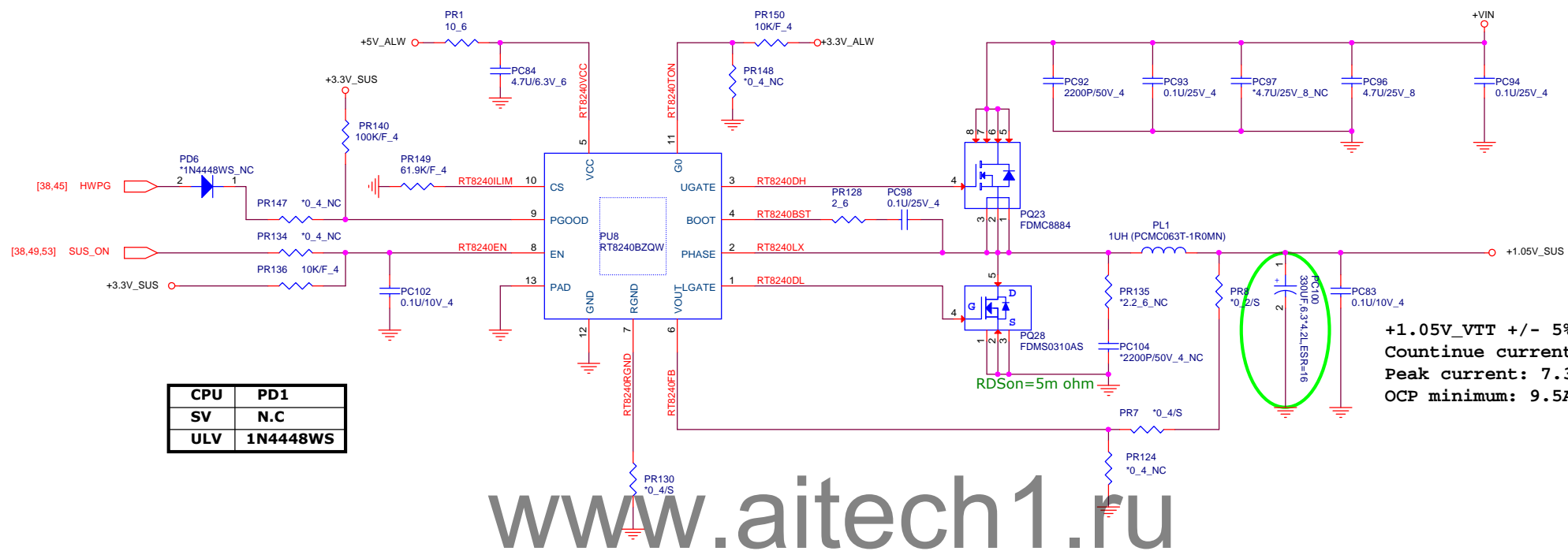


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|   |                        |                             |                |
|---|------------------------|-----------------------------|----------------|
|  |                        | <b>Quanta Computer Inc.</b> |                |
|   |                        | <b>PROJECT : JW8B</b>       |                |
| Size  | Document Number        |                             | Rev            |
|   | NC                     |                             | A              |
| Date:   | Tuesday, June 18, 2013 |                             | Sheet 48 of 57 |



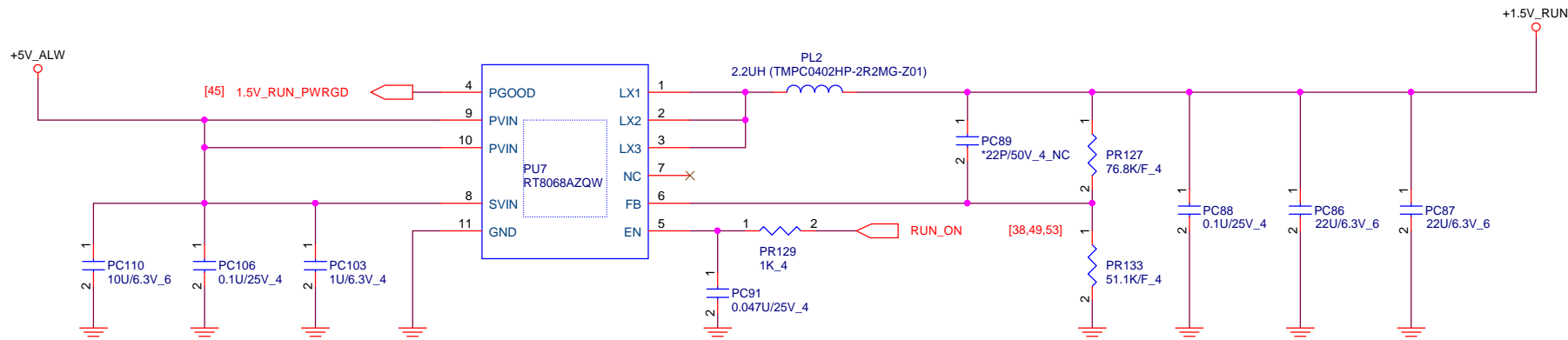




**+1.05V\_VTT +/- 5%**  
**Countinue current: 5A**  
**Peak current: 7.3A**  
**OCp minimum: 9.5A**

|     |          |
|-----|----------|
| CPU | PD1      |
| SV  | N.C      |
| ULV | 1N4448WS |

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**+1.5V\_RUN**  
 1.5 Volt +/- 5%  
 Fsw : 1MHz  
 TDC : 1A  
 Max : 1.5A  
 OCP :3A

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**PROJECT : JW8B**

|      |                               |     |
|------|-------------------------------|-----|
| Size | Document Number               | Rev |
|      | <b>+1.5V_RUN (RT8068AZQW)</b> | 1A  |

Date: Tuesday, July 09, 2013 Sheet 51 of 57

For 15W 1phase change item  
 PR20 499k → CS44992FB11  
 PR166 348k → CS43482FB16  
 PR170 75k → CS37502FB12  
 PR123 1.6k → CS21602FB00  
 PR164 63.4k → CS36342FB11

For 28W 1phase change item  
 PC132, PC133, PC134 → CH6221M9900  
 PR20 392k → CS43922FB17  
 PR166 360k → CS43602FB00  
 PR170 100k → CS41002FB28  
 PR123 1.65k → CS21652FB29  
 PR164 33.2k → CS33322FB13

For 2 phase → NC  
 For 1 phase → Short

